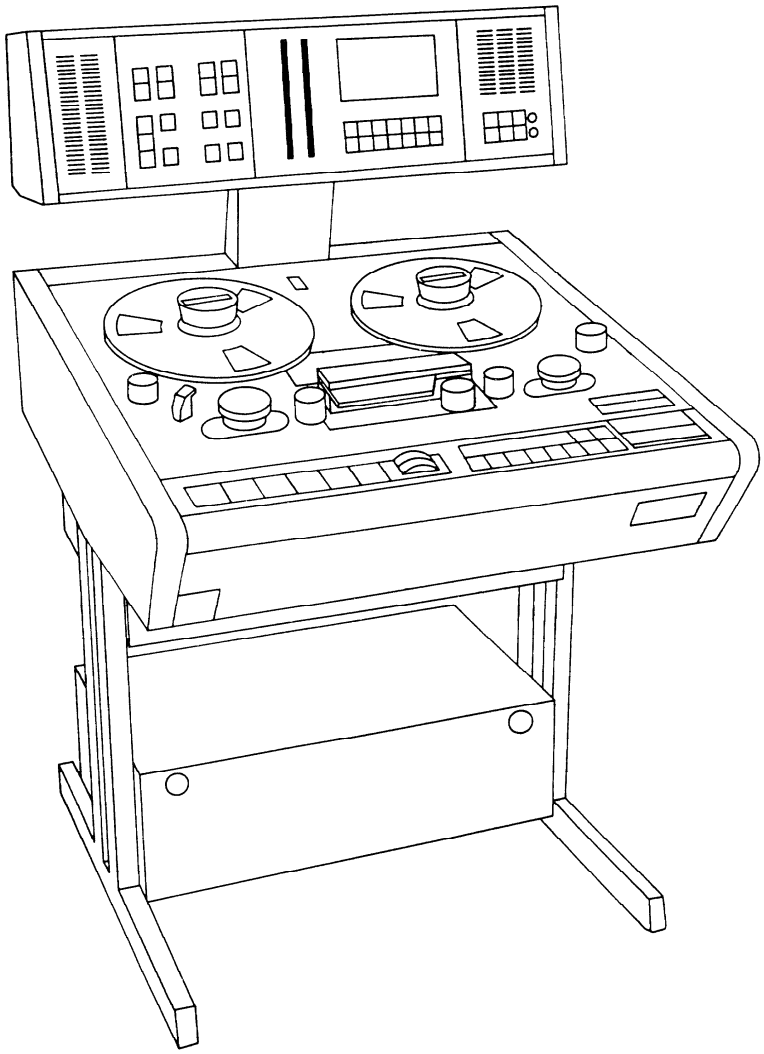
STUDER D820 X

Professional Digital Master Recorder

Operating Instructions



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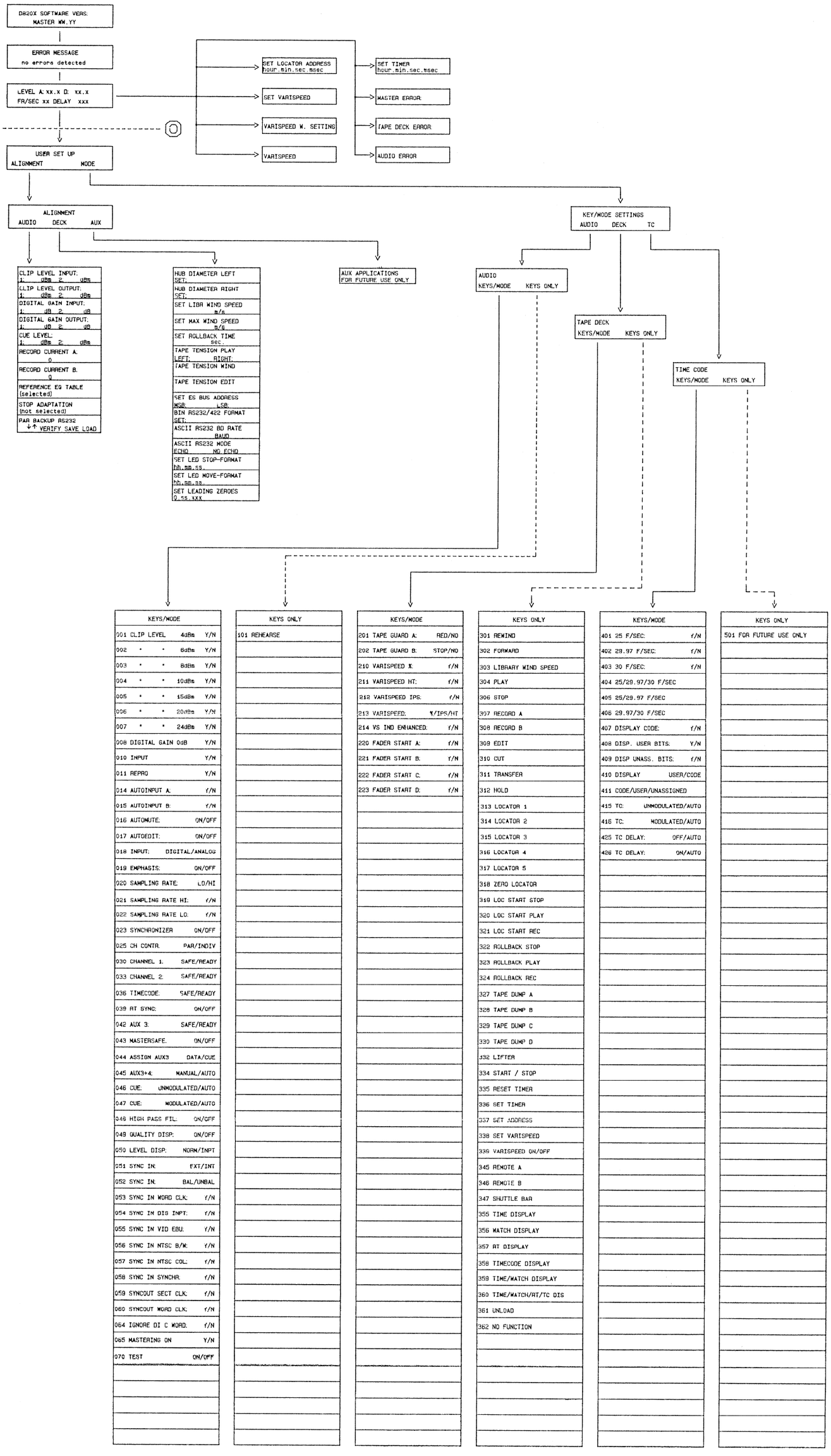
D820X MENU STRUCTURE



KEYS/MODE	
001 CLIP LEVEL	4dBm Y/N
002 " "	6dBm Y/N
003 " "	8dBm Y/N
004 " "	10dBm Y/N
005 " "	15dBm Y/N
006 " "	20dBm Y/N
007 " "	24dBm Y/N
008 DIGITAL GAIN	0dB Y/N
010 INPUT	Y/N
011 REPRO	Y/N
014 AUTOINPUT A:	Y/N
015 AUTOINPUT B:	Y/N
016 AUTOMUTE:	ON/OFF
017 AUTOEDIT:	ON/OFF
018 INPUT:	DIGITAL/ANALOG
019 EMPHASIS:	ON/OFF
020 SAMPLING RATE:	LO/HI
021 SAMPLING RATE HI:	Y/N
022 SAMPLING RATE LO:	Y/N
023 SYNCHRONIZER	ON/OFF
025 CH CONTR.	PAR/INDIV
030 CHANNEL 1:	SAFE/READY
033 CHANNEL 2:	SAFE/READY
036 TIMECODE:	SAFE/READY
039 AT SYNC:	ON/OFF
042 AUX 3:	SAFE/READY
043 MASTERSAFE:	ON/OFF
044 ASSIGN AUX3	DATA/CUE
045 AUX3+4:	MANUAL/AUTO
046 CUE:	UNMODULATED/AUTO
047 CUE:	MODULATED/AUTO
048 HIGH PASS FIL.	ON/OFF
049 QUALITY DISP:	ON/OFF
050 LEVEL DISP:	NORM/INPT
051 SYNC IN:	EXT/INT
052 SYNC IN:	BAL/UNBAL
053 SYNC IN WORD CLK:	Y/N
054 SYNC IN DIG INPT:	Y/N
055 SYNC IN VID EBU:	Y/N
056 SYNC IN NTSC B/W:	Y/N
057 SYNC IN NTSC COL:	Y/N
058 SYNC IN SYNCHR.	Y/N
059 SYNCOUT SECT CLK:	Y/N
060 SYNCOUT WORD CLK:	Y/N
064 IGNORE DI C WORD:	Y/N
065 MASTERING ON	Y/N
070 TEST	ON/OFF

KEYS ONLY
101 REHEARSE

KEYS/MODE	
201 TAPE GUARD A:	RED/NO
202 TAPE GUARD B:	STOP/NO
210 VARISPEED %:	Y/N
211 VARISPEED HT:	Y/N
212 VARISPEED IPS:	Y/N
213 VARISPEED:	%/IPS/HT
214 VS IND ENHANCED:	Y/N
220 FADER START A:	Y/N
221 FADER START B:	Y/N
222 FADER START C:	Y/N
223 FADER START D:	Y/N

KEYS ONLY
301 REWIND
302 FORWARD
303 LIBRARY WIND SPEED
304 PLAY
306 STOP
307 RECORD A
308 RECORD B
309 EDIT
310 CUT
311 TRANSFER
312 HOLD
313 LOCATOR 1
314 LOCATOR 2
315 LOCATOR 3
316 LOCATOR 4
317 LOCATOR 5
318 ZERO LOCATOR
319 LOC START STOP
320 LOC START PLAY
321 LOC START REC
322 ROLLBACK STOP
323 ROLLBACK PLAY
324 ROLLBACK REC
327 TAPE DUMP A
328 TAPE DUMP B
329 TAPE DUMP C
330 TAPE DUMP D
332 LIFTER
334 START / STOP
335 RESET TIMER
336 SET TIMER
337 SET ADDRESS
338 SET VARISPEED
339 VARISPEED ON/OFF
345 REMOTE A
346 REMOTE B
347 SHUTTLE BAR
355 TIME DISPLAY
356 WATCH DISPLAY
357 AT DISPLAY
358 TIMECODE DISPLAY
359 TIME/WATCH DISPLAY
360 TIME/WATCH/AT/TC DIS
361 UNLOAD
362 NO FUNCTION

KEYS/MODE	
401 25 F/SEC:	Y/N
402 29.97 F/SEC:	Y/N
403 30 F/SEC:	Y/N
404 25/29.97/30 F/SEC	
405 25/29.97 F/SEC	
406 29.97/30 F/SEC	
407 DISPLAY CODE:	Y/N
408 DISP. USER BITS:	Y/N
409 DISP UNASS. BITS:	Y/N
410 DISPLAY	USER/CODE
411 CODE/USER/UNASSIGNED	
415 TC:	UNMODULATED/AUTO
416 TC:	MODULATED/AUTO
425 TC DELAY:	OFF/AUTO
426 TC DELAY:	ON/AUTO

KEYS ONLY
501 FOR FUTURE USE ONLY

Table of Contents Section 1: General References

1 General References

1.1 Quick Reference Description

General Overview

The analog family of STUDER recorders serves as "workhorses" in recording studios all over the world since many years. The D820X continues this tradition into the digital age. STUDER has decades of experience in audio recorder design and all of this experience and craftmanship is incorporated in the D820X. It is a very stable and reliable recorder offering many novel features. The D820X demands no radical departure from the well proven operating conditions established with recorders in the analog era. In every aspect it fits neatly within an analog or digital environment and provides major improvements over competitive products. The D820X is a "no frills" design offering ease of handling and servicing, high reliability and superb sonic quality. In short: proven STUDER quality.

The D820X is a digital open-reel recorder with two main (digitalaudio) channels and four auxiliary tracks. It has been designed according to the DASH format (DASH stands for "Digital Audio Stationary Heads") which is also supported by MATSUSHITA, SONY and TEAC-TASCAM. The digitalaudio channels specifically operate according to the DASH-Twin format. Each audio channel is recorded onto four tracks to ensure robust data recording and playback performance and the tape speed is 15 ips. at 48 kHz sampling frequency for improved cueing accuracy.

The Twin format offers the ultimate in recording reliability: the loss of any track (in the D820X even of the reference track) causes no degradation of audio quality or reliability. Across-the-tape data loss of up to 39 mm and tape splices are handled error- and concealment-free.

The D820X is essentially a two channel recorder with stationary heads and 12 tracks on 1/4" wide tape. The playing time is 2 hours plus with 14" reels. The main channels provide a capacity of 16 bits per audio sample word and the use of emphasis (15 + 50 µsec.) is optional. Two different sampling frequencies are standard and a third (44.056 kHz) is offered optional. Off-tape monitoring is possible in all modes.

The D820X is equipped with the type 820 tape deck which is famous for its fast access time (15 m/sec. spooling time) and smooth tape handling. The transport features up to five address locators and a zero locator. It locates to the last start address with succeeding play, record or stop function. Programming of the D820X is menu driven and the user is guided by messages which indicate the state of the recorder in plaintext. Sophisticated synchronization facilities as well as adjustment-free playback electronics are also among the many outstanding characteristics of this recorder.

Two independent channels for digital audio are provided with analog and digital in- and outputs. There are four remaining tracks: the first auxiliary track (from below) is a dedicated time code track. The D820X has a built-in time code reader and display and locates to time code with an (optional) autolocator. The time code track is aligned at the output with digital audio. The neighbouring auxiliary track is the reference time track. It offers cueing accuracy with sample resolution and is used to record format and tape specific information (sampling frequency, version, etc.). A built-in generator, reader and display is provided for the reference time track. Its output is aligned with digital audio and time base corrected. The two auxiliary tracks on top of the head may be configured to store one or two cue channels. In mono (aux4mix) mode both digitalaudio channels are mixed to one track and the other is a free data track with 50 kHz bandwidth for storage of subcode or similar information.

1.2 Versions

		Order Number
Basic Version 1.861.022.00		**60.218.20501**
Consisting of:	• tape deck, console or rack mounting, with overbridge	1.861.080
	• electronics box	1.861.320
	• headblock D820X	1.050.116
	• overbridge, containing monitor panel	1.861.365
	display panel	1.861.555
	and channel control panel	1.861.370
Standard Features:	• 14" max. reel diameter capacity	
	• 44.1/48 kHz sampling frequencies	
	• built-in time code reader	1.861.761
	• parallel remote control port	1.820.738
	• parallel synchronizer port	1.820.738
	• port for external display panel	
	• analog input without transformer	1.861.752
	• analog output without transformer	1.861.751
	• mechanical elapsed time counter	1.820.861
	• connector configuration: USA (input female, output male)	
	• built-in scissors and splicing block	
	• NAB adapters included (pair)	1.013.344.00
	• power cord IEC-320, 16A, 3 m	10.223.001.13
	• set of fuses included	
	• set of key labels included (secondary keyboard and service keyboard)	
	• set of status display labels included	
	• set of connectors included	
	• set of tools included	
	• one empty reel included, AMPEX, 14"	
	• one virgin tape Ampex 467, 14"	
	• operating and service manuals (e) included, 3 volumes	10.27.0610

Standard Accessories

	Order Number
• power cord IEC-320, 16A, 3 m	10.223.001.13
• set of fuses	
• set of key labels, secondary keybd. & servicing keybd.	
• set of connectors	
• set of tools	
• set of precision reels	
• splicing block	
• splicing tape, suitable for digital audio tape	
• operating and service manuals (e), volumes I, II, III	10.27.0610
• operating manual (e), volume I	10.27.0580
• circuit diagrams, volume II	10.27.0590
• servicing manual, volume III	10.27.0600
• connector to parallel remote port, DSub25	20.020.303.16
• connector to synchronizer control port, DSub25	20.020.303.15

1.3 Options

		Order Number
USA connector configuration (acc. to IEC 268-12)		**20.861.420.00**
consisting of:	connectorfield trafo USA	1.861.777.00
	connectorfield cue USA	1.861.586.00
	mounting panel no. 6 (rack)	1.861.586.02
	label cue USA	1.861.586.03
	label box USA	1.861.320.12
	mounting accessories	
EURO connector configuration		**20.820.421.00**
consisting of:	connectorfield EURO	1.861.773.00
	(3 PCB needed per box)	
	connectorfield USA (DI/DO)	1.861.775.11
	connectorfield cue EURO	1.861.774.00
	mounting panel box	1.861.320.11
	mounting panel no. 6 (rack)	1.861.586.02
	label cue EURO	1.861.586.03
	label box EURO	1.861.320.12
	cover for XLR	1.820.560.11
	mounting accessories	
Analog input w/o transformers		**1.861.752.23**
Analog input with transformers		**20.820.426.00**
Timing + Test board 1.861.063 for 48/44.1 kHz sampling frequencies		**20.861.861.20**
consisting of:	Timing + Test board	1.861.862.20
	VCXO 48/44.056	1.861.701.00
	Dual PLL	1.861.725.00
	Composite Video	1.861.720.00
	mounting accessories	
Timing + Test board 1.861.064 for 48/44.056 kHz sampling frequencies		**20.820.435.00**
consisting of:	Timing + Test board	1.861.862.20
	VCXO 48/44.056	1.861.701.00
	Dual PLL	1.861.725.00
	Composite Video	1.861.720.00
	mounting accessories	
Timing + Test board 1.861.065 for 44.1/44.056 kHz sampling frequencies		**20.820.436.00**
consisting of:	Timing + Test board	1.861.862.20
	VCXO 44.1/44.056	1.861.702.00
	Dual PLL	1.861.725.00
	Composite Video	1.861.720.00
	mounting accessories	

Conversion kit for basic Timing + Test board for 48/44.056 kHz sampling frequencies		**20.861.435.00**
consisting of:	VCXO 48/44.056 (plug-in board)	1.861.701.00
Conversion kit for basic Timing + Test board for 44.1/44.056 kHz sampling frequencies		**20.861.436.00**
consisting of:	VCXO 44.1/44.056 (plug-in board)	1.861.702.00
Dust cover tape deck and panel, plastic		**1.058.001.11**
Dust cover tape deck, plastic		**1.058.001.10**
Serial interface, single RS-232 format for use with TLS 4000, Mk.II		**20.820.342.00**
consisting of:	serial remote controller	1.810.751.81
	ribbon cable, 0.55 m with connectors	1.023.190.05
	mechanical parts	1.010.032.54
	Connector to serial interface RS-232, DSub9	20.020.303.07
Serial interface STUDER for serial controller and remote timer		**20.820.345.00**
consisting of:	serial remote interface	1.820.729.20
	ribbon cable, 10 pin, 0.2 m	1.023.150.02
	mechanical parts	1.010.032.54
	Connector to serial controller & rem. timer, DSub9	20.020.303.20
	Connector to synchronizer control port, DSub25	20.020.303.15
	Connector to parallel tape transport port, DSub25	20.020.303.16
	Connector to Display panel, test or ext. clk, DSub25	20.020.303.10
Rear panel tape deck w/o neck		**1.820.090.12**
Overbridge with shelve		**20.820.348.00**
consisting of:	rear panel tape deck with neck	1.820.550.08
	overbridge with shelve	1.820.572.00
	mounting accessories	

1.4 Accessories

		Order Number
External display panel with 15m cable, 170mm height		**1.861.056.00**
consisting of:	display panel	1.861.555.00
	consisting of:	
	keyboard display	1.861.741.00
	display processor	1.861.742.23
	frontpanel display panel	1.861.555.02
	cable round, 15 m with DSub25	1.023.751.00
Display panel, 190mm module, 15m cable		**1.861.057.00**
consisting of:	keyboard display	1.861.741.81
	display processor	1.861.742.23
	frontpanel display panel, 190 mm	1.861.555.10
	cable round, 15 m with DSub25 mounting accessories, window, filter, etc.	1.023.751.00
External display panel in table top cabinet, 170mm		**1.861.061.00**
consisting of:	display panel	1.861.556.00
	consisting of:	
	keyboard display	1.861.741.81
	display processor	1.861.742.23
	frontpanel display panel	1.861.555.02
	cable round, 15 m with DSub25	1.023.751.00
	case for display panel	1.328.210.10
	side panel left	1.328.210.01
	side panel right	1.328.210.02
	ribbon cable, 0.42 m	1.023.362.04
	mounting plate for connector	1.328.210.11
	foot for cabinet (4 pcs. needed) mounting accessories	31.02.0211
Parallel remote control cabinet with 15 m cable, DSub25 connector		**20.820.366.00**
Parallel remote control module with 15 m cable, DSub25 connector		**20.820.367.00**
Pass-through connector DSub25		**21.328.254.00**
	for additional parallel control functions (faderstart, etc.) for installation into parallel remote control cabinet	20.820.366.00
Serial remote control cabinet with 15 m cable, DSub9 connectors & special label set		**1.861.058.00**
	(OPTION 20.820.345.00 required)	
Serial remote control module with 15 m cable, DSub9 connectors & special label set		**1.861.059.00**
	(OPTION 20.820.345.00 required)	
Serial remote counter		**1.861.060.00**
	(OPTION 20.820.345.00 required) for desk top use or installation into mounting frame 1.328.270.31/32/33, with 15m cable, DSUB9 connectors & special label set	
Mounting frame		**1.328.270.31**
	with mounting positions for installation of one 1.861.060.00 serial remote counter	

Mounting frame		**1.328.270.32**
	with mounting positions for installation of two 1.861.060.00 serial remote counters	
Mounting frame		**1.328.270.33**
	with mounting positions for installation of three 1.861.060.00 serial remote counters	
Table cabinet, fitting 6 STUDER standard modules		**1.328.095.00**
	Remote control module for installation, STUDER standard module (1E) size	20.820.367.00
Filler panels for table cabinet, 190 mm height		
	1 module width, anodized finish	1.038.341.00
	2 modules width, anodized finish	1.038.342.00
	3 modules width, anodized finish	1.038.343.00
	1 module width, gray paint finish	1.328.185.00
	2 modules width, gray paint finish	1.328.186.00
	3 modules width, gray paint finish	1.328.187.00
	5 modules width, gray paint finish	1.328.189.00
Consoles		
	Consoles with traverse height 840 mm, with castors	20.020.205.45
Reel adaptors, NAB prof., with aluminium hand piece, 1/4", 1pcs		**1.013.344.00**
Cine adaptor, 1/4", 1pcs.		**1.013.347.00**
NAB Metalreel, empty, 1/4" (10.5")		**10.213.001.01**
NAB Metalreel, empty, 1/4" (14")		**10.353.001.03**

1.5 Servicing Aids

	Order Number
Basic tool case with soldering iron and demagnetizer 110 V	20.020.001.20
Basic tool case with soldering iron and demagnetizer 220 V	20.020.001.21
Additional tool set D820X, excl. extender boards	20.020.001.37
39-pole extender board, EURO format, for rack electronics (identical to A820)	1.820.799.00
64-pole extender board, EURO format, for tape deck electronics (identical to A820)	1.228.324.81
96-pole extender board, EURO format, for auxiliary rack and cage electronics	1.228.325.00
96-pole extender board, for digital electronics (box) 4pcs. required	1.861.779.00

Supported terminal drivers

1	ASCII	simple ASCII
2	ESPRIT	esprit terminals by Hazeltine
3	HP	Hewlett-Packard terminals
4	TVI905	Televideo 905 terminal
5	ANSI	several manufacturers (e.g. IBM-PC)

Splicing tape, suitable for digital audio tape
Recommended type: PPI-3883 (available through Studer International)

Marking pen, suitable for digital audio tape
Recommended types: fluorescent pens

Cleaning fluid
Recommended types: aethylene alcohol, or Kaltron 113 MDR ($C_2Cl_3F_3$)

IEC Primary Reference Tape for Digital Audio
AMPEX, Production No. 8000

Operating and service manuals (e), volumes I, II, III	10.27.0610
Operating manual, volume I (e)	10.27.0580
Circuit diagrams, volume II (e)	10.27.0590
Servicing manual, volume III (e)	10.27.0600

1.6 Technical Specifications

Power Consumption	D820X equipped with all panels but without remotes.		
	In STOP mode:		≤ 380 VA
	In PLAY mode:		≤ 380 VA
	In RECORD mode:		≤ 400 VA
	In WIND mode:		≤ 550 VA
	Power-up:		≤ 850 VA
	Recommended mains power, for worst case operation:		900 VAp
Power Supply	(with supply voltage selector) 100 V ... 140 V or 200 V ... 240 V; ±10%; 50 or 60 Hz For conversion to 100 V mains voltage, detailed instructions are available from STUDER representatives.		
Disturbed Operation	The operating status is unaffected by line voltage failures up to 100 msec.		
Ambient Temperature Range	0 ... 40° centigrade (+32 ... +104° F)		
Relative Humidity	20 ... 90 %, non-condensing		
Safety Standard	According to IEC recommendation, publication 65, degree of protection: I. Line filter, power switch, power fuse, power transformers and line voltage selector conform to type I and II.		
Dimensions	**Height:**	console with castors:	840 mm
		console with floor slides:	780 mm
		height of normal panel:	336 mm
		height of panel with TLS4000 LCU overbridge:	388 mm
	Width:	without 14" reels:	700 mm
		with 14" reels:	750 mm (approx.)
	Depth:	transport horizontal:	700 mm (approx.)
Weight	Version with panel and console with castors (height = 840 mm): 122 kg		
Tape Speed	15.0 ips. (0.381 m/sec.)		for 48 kHz sampling frequency
	13.78125 ips. (0.35 m/sec.)		for 44.1 kHz sampling frequency
	13.76748 ips. (0.34969 m/sec.)		for 44.056 kHz sampling frequency
Tape Speed Deviation	± 0.2% maximum		
Tape Slip	0.1% maximum		
Wow and Flutter	Time base corrected tracks (digitalaudio, reference time):		unmeasurable
	Not time base corrected tracks (time code, cue, aux3):		0.04% max.
	The latter are measured with peak weighting according to DIN 45507 or IEC publication 386, respectively. Ambient temperature 0 ... 40° centigrade (32 ... 104° F).		
Tape Reels	NAB, CINE, DIN max. diameter 356 mm (14 in.), min. hub diameter 45mm (1.77 in.)		

Start Time

450 ... 500 msec. at 48 kHz (15 ips.) and 1400 m tape on NAB reel (10.5 ") for unmeasurable flutter values.

650 ... 700 msec. for identical conditions as above, but with unknown tape inertia parameters (see chapter 2.5.6: "Reproduce").

Composition of start time:			
command master - tape deck:		5 msec.	
processing time tape deck:		10 msec.	
ramp :		200 msec.	
command tape deck - master:		40 msec.	(polling, status update)
processing time master:		10 msec.	
command master - syscon:		5 msec.	
processing time syscon:		5 msec.	
timing jitter for all above:			± 25 msec.
interleave:	119 blocks		
odd-even delay:	204 blocks		
tbc:	4 blocks		
decoder:	73 blocks		
	---		
total hardware	400 blocks:	200 msec.	at 48 kHz

other minor delays (filter, start delay transformatter, etc.) are not considered.

Tape Selection

Four brands can be recommended at this time:

AMPEX 467, SONY D-1/4-1460, 3M 275 and Maxell PC27-10B.
The recording current settings A and B should be set to 0 for all types.

The performance of the recorder in terms of block eror rate, dropouts, etc. depends strongly on the adjustment of the write currents. The adjustment procedure is described in this operating manual (par. 3.5: Service Adjustments). The currents have been matched to a specific headblock assembly and are factory adjusted for each track separately to ensure optimum performance and compatibility. The D820X allows for two individual offset settings via commands from the menu to accomodate vastly different tape brands.

Do not change the individual recording current settings of the write amplifier!

It is strongly recommended not to demagnetize the heads!

Inadequate demagnetizers (Handymag, etc.) may easily have a detrimental effect. The D820X is shipped with carefully demagnetized heads.

Tape Timer

9-digit LED, indicating hours, minutes, seconds and milliseconds/frames (valid for all tape speeds). Counts past zero with leading negative sign.

Range: -9 h 59 min. 59.999 sec. to 23 h 59 min. 59.999 sec.

Software controlled function to suppress leading zeroes (menu driven). Software controlled function to set stop and move display format (menu driven). Displays absolute time derived by move roller, relative time derived by move roller in watch mode and time addresses from the time code or reference time track.

Reset and stop functions.

Winding Speed	Programmable, from 4 ... 590 ips. (0.1 ... 15 m/sec.). Selectable automatic speed reduction at the tape ends (tape guard function).	
Winding Speed	Approximately 90 sec. for 1000 m tape; approx. 55 sec. for 762 m tape.	
Stopping Time from Spooling	Approximately 4 seconds with full 1000 m - reel from maximum winding speed.	
Analogaudio Inputs	Input w/o transformer (1.861.752)	
	Maximum input level:	24 dBV.7
	Minimum input level for rated output:	4 dBV.7
	Input impedance, symmetrically driven:	>20 kΩ (audio range)
	Input impedance, one side grounded:	>10 kΩ (audio range)
	Common-mode rejection ratio:	>70 dB (10 ... 1000 Hz)
	Common-mode rejection ratio:	>50 dB (<20 kHz)
	Maximum common-mode voltage:	50V
	Input with transformer (1.861.753)	
	Maximum input level:	24 dBV.7
	Minimum input level for rated output:	4 dBV.7
	Input impedance, symmetrically driven:	>10 kΩ (audio range)
	Input impedance, one side grounded:	>10 kΩ (audio range)
	Common-mode rejection ratio:	>80 dB (20 ... 1000 Hz)
	Common-mode rejection ratio:	>60 dB (1 ... 16 kHz)
	Maximum common-mode voltage:	100V
Analogaudio Output	Maximum output level, symmetrical load:	24 dBV.7
	Maximum output level, unsymm. load:	20 dBV.7
	Minimum output level:	4 dBV.7
	Maximum output impedance:	40 Ω
	Common-mode rejection ratio:	>85 dB (10 ... 1000 Hz)
	Common-mode rejection ratio:	>65 dB (<20 kHz)
	Maximum applied common-mode voltage:	80 VDC through 600 Ω
	Limit load conditions, capacitive:	100 nF

Overall Analogaudio Specifications (A-to-D and D-to-A Cascaded)

Frequency response:	10 ... 23000 Hz
Maximum ripple:	± 0.5 dB (<19 kHz)
Aliased output components from out-of-audio-band input components, sampling frequency = 44.1 kHz:	<-60 dB (>29 kHz)
Phase deviation from linearity:	<0.5*f degrees (f[kHz])
Crosstalk:	>75 dB (1 kHz/20 kHz)
THD+N, full scale signal (*):	>84 dB (10 ... 17000 Hz), 20dBV.7
THD+N, full scale signal (*):	>83 dB (10 ... 17000 Hz), 0dBV.7
THD+N, 30 dB below maximum level (*):	>55 dB (10 ... 17000 Hz)
THD+N, 60 dB below maximum level (*):	>25 dB (10 ... 17000 Hz)
Idle channel noise (*):	>85 dB
THD+N, full scale signal (**):	>88 dB (10 ... 17000 Hz)
THD+N, 30 dB below maximum level (**):	>60 dB (10 ... 17000 Hz)
THD+N, 60 dB below maximum level (**):	>30 dB (10 ... 17000 Hz)
Idle channel noise (**):	>88 dB

(*) = no emphasis used
(**) = with emphasis

Note: Overall specifications with 1.861.753:

THD+N, full scale signal:	>84 dB (50 ... 17000 Hz), 20dBV.7

Analogaudio Output Specifications (Input Digital)

Frequency response:	10 ... 23000 Hz
Maximum ripple:	± 0.5 dB (<19 kHz)
Phase deviation from linearity:	<0.5*f degrees (f[kHz])
Crosstalk:	>90 dB (1 kHz/20 kHz)
THD+N, full scale signal (*):	>90 dB (10 ... 20000 Hz), 20dBV.7
THD+N, full scale signal (*):	>88 dB (10 ... 20000 Hz), 0dBV.7
THD+N, 30 dB below maximum level (*):	>58 dB (10 ... 20000 Hz)
THD+N, 60 dB below maximum level (*):	>28 dB (10 ... 20000 Hz)
Idle channel noise (*):	>95 dB
THD+N, full scale signal (**):	>88 dB (10 ... 20000 Hz)
THD+N, 30 dB below maximum level (**):	>60 dB (10 ... 20000 Hz)
THD+N, 60 dB below maximum level (**):	>30 dB (10 ... 20000 Hz)
Idle channel noise (**):	>90 dB

(*) = no emphasis used
(**) = with emphasis

Measurement Conditions

- Input CMRR measured with an equivalent noise bandwidth of 45 kHz.
- Output CMRR measured according to ARD recommendations at 20 dBV.7 with 300 Ω load, highpass 400 Hz, lowpass 80 kHz, single pole.
- Output level measured with 600 Ω load.
- Crosstalk: one channel idle, one channel active, full scale signal, gains maximum.
- THD+N: measured over an equivalent noise bandwidth of 26 kHz.
  Emphasis on: the amplitude of the input signal source should follow an inverse pre-emphasis characteristic.
- Idle channel noise: no signal applied, equivalent noise bandwidth = 45 kHz.
- dBV.7: absolute voltage level re 0.775V.
- See appendix to Test Report delivered with each recorder for more detailed information.

Sampling Frequencies

Standard:	48 and 44.1 kHz
Optional:	44.056 kHz
Frequency accuracy:	less than ± 10 ppm

Emphasis

Selectable 15/50 µsec. Dual channel operation. CCITT J17 emphasis transparent from digital input to digital output in all tape deck modes except PLAY and RECORD.

Digitalaudio Format

Recording format:	Twin DASH (each track recorded twice and each sample with 204 blocks distance)
No. of tracks per channel:	4, identically formatted
Bit rate:	576 kb/sec.
Error correction code:	Cross-Interleave plus Cyclic Redundancy Check
Redundancy per track:	33.3% (CIC)
Interleave distance:	119 + 204 blocks
Correctability:	up to triple errors
Bursterrorlength for perfect correction:	39 mm (204 blocks) loss of all tracks
Trackloss behavior for arbitrary dropout length	
loss of one track per CH:	perfect correction
loss of two tracks/CH:	perfect correction or second order interpolation (depending on track number)
loss of three tracks/CH:	first order interpolation
loss of Reference track:	no influence for a stereo recording
Modulation code:	HDM-1
Lineal data density:	1.512 Mb/m/track (38400 bit per in. per trk)
Transition density:	1.008 Mb/m/track (25600 fcpi/track)
Min. recorded wavelength:	1.984 µm

Digitalaudio In- and Outputs

According to standard AES3-1985, ANSI S4.40-1985 CEI/IEC 958 ("professional AES/EBU format"). When the control word follows the consumer format, only the emphasis flag is considered in override disable mode. See par. 1.7: Interfacing Specifications.

Spread of locking time from SR-VRSPD = 6 kHz (synchronizer port) to digital input: 350 ... 600 milliseconds.

Digitalaudio Performance

Resolution:	16 bit, linear
Blocking structure:	
delay in read after write mode:	234 blocks
encoder delay	4 blocks
formatter delay	1 block
head distance	152 blocks
TBC delay	4 blocks
decoder delay	73 blocks

The figures above and below are given for the first sample at encoding/ decoding. For a center sample add 161.5 blocks to the encoding and decoding process.

delay in INPUT mode:	8 words (also local REHEARSE)
delay in REHEARSE mode:	82 blocks (EE-loop 2)

Locking to integer multiples of the incoming wordsync.

Input gain adjustment:	-10/+6 dB in 0.1 dB increments
Output gain adjustment:	-10/+6 dB in 0.1 dB increments
Max. blockerror rate:	(first recording) 100 ppm per track(*) (overwritten) 200 ppm per track (*)

(*) Factory specification.

Crossfiltering Time

18 blocks linear.

Absolute time:	9 msec. at 48 kHz
or	9.8 msec. at 44.1 kHz

Due to the splice constraints A and B (see below) variable crossfade times would become difficult to handle for the operator and have been omitted therefore.

Concealment

First and second order interpolations, mutings.

Strategy:

single error occasionally:	second order interpolation	(1)
single error continously:	first order interpolation	(2)
double error:	first order interpolation	(3)
triple error:	first order interpolation	(4)
more than triple error:	muting	

Error patterns:

(1) GGGXGGXGGG	G = reliable sample
(2) GXGXGXGXGX	X = interpolated sample
(3) GXXGGGXXGG	
(4) GXXXGGXXXG	

Signal Quality Display

Display per channel (8 LED's):

Normal operation.	
Second pass QP-parity correction.	
Fingerprint	(85 ... 204 blocks, ≥ 4 tracks).
Trackloss	(≥ 512 blocks, ≥ 1 track).
Second order interpolation	(quadratic).
First order interpolation	(linear).
Muting	(timeout = 0.5 sec.).
No data.	

Priority encoded. The more severe error is displayed.

Tape Cut Performance

No concealment is required for carefully made splices.
Splice detection does not rely on the reference track. Applied methods: occurence and location of block sync words, continuity of block addresses, detection of interleave errors. With RT SYNC mode: interleave errors only.

Tape Cut Constraints

- Minimum length of tape to be cut out for the event to become inaudible: 18 blocks.
- Distance by which a cut out peace of tape should be elongated: 9 blocks at both ends. Otherwise it may become audible in the crossfade area (2 * 9 blocks).
- Minimum distance before a new splice can be processed: 187 blocks.
- Minimum distance between splices for (theoretically) full correction: 221 blocks.

Punch-In/Out Performance

"Hard" punches with crossfade at playback.

Max. delay:	1 block
Unreliable data:	1 block

Due to the two head configuration, accurate punches regarding timing are to be made via autolocator or electronic editor rather than "on the fly".

Cue Track Performance

Modulation:	PDM, mod. index = 0.7
Demodulation:	PDM/unmodulated/auto
Frequency response record-reproduce:	50 Hz ... 10 kHz +1/-3dB
Signal-to-noise ratio record reproduce	
Linear, RMS, 30 Hz ... 20 kHz:	better than 60 dB
A weighted, RMS, according to IEC publ. 179:	better than 64 dB
Total harmonic distortion and noise at 1 kHz:	less than 2% (*)
Crosstalk attenuation at 1 kHz:	better than 60 dB
Erase efficiency (**):	better than 60 dB
Overwrite attenuation (***):	better than 36 dB
Erase and bias frequency:	none
Speed range:	1/5 ... 5 times nom. speed
Outputs:	see interfacing specs

(*) measured 10 dB below full scale
(**) 1 kHz erased, residual signal measured selectively
(***) 1 kHz overwritten with 100 Hz

Auxiliary 3 Track Performance

Data track only (in AUX4MIX mode).

Bandwidth (-3 dB):	10 Hz ... 50 kHz
Interfacing specifications:	see par. 1.7

Time Code Track Performance

Code format: accepts longitudinal SMPTE/EBU (ES), 80 bit address code. Input delay for accurate alignment with digtalaudio.

Time code is always recorded with PDM modulation, demodulation is selectable for modulated or unmodulated recordings respectively, or according to a flag on the reference time track in automatic mode.
The time code input is not linked with the videoclock input.
The TC output (biphase) is aligned with digitalaudio (no phaselock) when an appropriate delay is activated.
The delay in reproduction mode is selectable to 25, 29.97 or 30 frames/second. In auto mode, the delay is active when in PLAY (or RECORD) mode. The line output and the display are then coincident with digitalaudio data. It is not active (no delay) in STOP or EDIT mode. The local or remote readout of TC data coincides with cue audio signals. STUDER synchronizers normally override the auto mode and desactivate the internal delay.
Speed range for built-in time code reader: ca. 0.007 ... 0.7 m/sec.
In- and outputs: see par. 1.7: Interfacing Specifications.

Reference Time Track Output

Built-in generator and reader. Display: see "TAPE TIMER".

Format:
according to the DASH reference time track format, serial data. Time base corrected and aligned with digitalaudio data. No wow and flutter or jitter. It ensures sample resolution and accuracy for digtalaudio data.

Clock In- and Outputs

- Videoclock input:
  composite video/ composite sync or square wave, unsymmetrical on BNC connector, symmetrical according to RS-422 on DSUB25 connector, 50, 60/1.001, 60 fr./sec., ± 100 ppm
- Wordclock input:
  frequency according to internal crystal configuration ± 100 ppm, unsymmetrical on BNC connector (RS-423 or TTL, jumper selectable on Timing + Test board), symmetrical according to RS-422 on DSUB25 connector, square wave
- Wordclock output:
  frequency according to internal crystal configuration switchable wordclock/sectorclock, unsymmetrical on BNC connector (RS-423 or TTL, jumper selectable on Timing + Test board), symmetrical according to RS-422 on DSUB25 connector
- Sectorclock output:
  frequency = (500 * fs)/48000, square wave switchable wordclock/sectorclock unsymmetrical on BNC connector (RS-423 or TTL, jumper selectable on Timing + Test board), symmetrical according to RS-422 on DSUB25 connector

Spread of audio muting time when switching from SR-VRSPD = 6 kHz (synchronizer port) to any sync source except digital input: 300 ... 450 milliseconds.
Spread od locking time from SR-VRSPD = 6 kHz (synchronizer port) to video EBU (worst case): 500 ... 1100 milliseconds.

Synchronizer Input

On parallel remote and synchronizer parallel connectors (DSUB25). Virtual input frequency = 9.6 kHz, the loop synchronizer-recorder automatically produces an offset frequency to 9.6 kHz according to the speed deviation in chase mode.

The D820X is supported by STUDER TLS 4000 Mk.II interfaces.
See par. 1.6: Interfacing Specifications for more information.

Remotes

1: parallel remote interface on DSUB25 connector
2: parallel synchronizer interface, DSUB25 connector
3: serial remote interface (DSUB9), RS-232, ASCII protocol (option)
4: serial remote interface (DSUB9), RS-422/232, ES protocol (option)
5: autolocator/remote timer interface, DSUB9, Studer bus (option)
6: interface for TLS4000 local control unit, DSUB9
5: external display panel connector, DSUB25, Sysbus

Terminal and Personal Computer Interfaces

- RS-232 interface (DSUB9) on transport for communication with master processor (with optional serial remote interface)
- RS-232 interface (DSUB25) on PCM box for communication with system controller

Both interfaces provide extensive remote control facilities, even of the internal local area network Sysbus) and diagnostic features for maintenance and tape analysis. Status, quality and gain overviews.

Display Panel

Calibrated gains (digital and analog) display. Uncalibrated gains (digital and analog) setting and display. Headroom (analog) setting and display. Accumulated peak level display readout in dB (resolution: 0.1 dB), with reset function.
Time (move roller, time code, reference time) display and reset function.
Watch (relative time) display, reset and stop functions.
Signal quality display.
Bargraph level display, digitally derived.

• Attack time :	sampling frequency
• Release time:	1.5 sec./20 dB
• Multiplexing:	≥ 50/sec.

Analog and digital clipping display.

Channel Control Panel	Safe/ready and input/repro settings for the digitalaudio channels, the time code track and the auxiliary track (if assigned). RT Sync function.
Monitor and Speaker Panel	Providing stereo monitoring facilities on the tape deck.

Note: 1 block corresponds to 0.5 msec. or 0.1905 mm (valid for 48 kHz sampling frequency)

1.7 Interfacing Specifications

1.7.1 Analogaudio CH1/2

Input without transformer coupling:	Input level range:	4 ... 24 dBV.7
	Max. input level:	24 dBV.7
	Input impedance:	>20 kΩ symmetrical,
		>10 kΩ one side grounded
	CMRR 20 ... 1000 Hz:	more than 70 dB
	Connector type:	XLR, pin 2 in-phase
Input with transformers:	Input level range:	4 ... 24 dBV.7
	Max. input level:	24 dBV.7
	Input impedance:	>10 kΩ
	CMRR 20 ... 1000 Hz:	more than 80 dB
	CMRR 1 ... 16 kHz:	more than 60 dB
	Connector type:	XLR, pin 2 in-phase
Output without transformer coupling:	Output level range:	4 ... 24 dBV.7 at 300 Ω load
	Max. output level:	26 dBV.7 symmetrical load
	Max. output level:	20 dBV.7 unsymmetrical load
	Output impedance:	less than 40 Ω
	Capacitive load:	up to 150 nF
	Output protection:	80 VDC max.
	Output symmetry:	better than 80 dB up to 10 kHz
	Connector type:	XLR, pin 2 in-phase

1.7.2 Auxiliary 3,4

AUX 3 input (data track only):	Bandwidth (-3dB):	10 Hz ... 50 kHz
	Input level range:	2 ... 10 V peak-to-peak
	Input impedance:	>600 Ω symmetrical,
		>300 Ω unsymmetrical
	Input coupling:	balanced, floating (transformer)
	Connector type:	XLR, pin 2 in-phase
AUX 3 output (in cue stereo mode):	Signal type:	cue right
	Output level range:	0 ... 20 dBV.7
	Max. output level:	22 dBV.7 into 300 Ω
	Output impedance:	less than 40 Ω (1 kHz)
	Output coupling:	balanced, floating (transformer)
	Capacitive load:	up to 100 nF
	Connector type:	XLR, pin 2 in-phase

AUX 3 output (in aux4mix mode):	Signal type:	data only
	Output level:	typ. 5.0 V peak-to-peak, fixed, bipolar
	Output coupling:	balanced, floating (transformer)
	DC content:	none
	Output impedance:	less than 40 Ω (1 kHz)
	Connector type:	XLR, pin 2 in-phase
AUX 4 output:	Signal type:	in cue stereo mode): cue left (in aux4mix mode): cue left and right

Specifications as AUX 3 output in cue stereo mode (see above).

1.7.3
Digitalaudio CH1,2

Input with transformer coupling (serial no. 1071 up):

According to AES3-1985, ANSI S4.40-1985, IEC/CEI 958:1989), except where otherwise noted.

Max. input voltage:	± 15 V
Input sensitivity:	± 0.5 V
Input impedance:	typ. 250 Ω, 100 Hz ... 6 MHz
Frequency accuracy:	sampling frequency ± 100 ppm (+)
Connector type:	XLR, pin 2 in-phase
AC coupling	
Validity bit:	not processed
User data:	not processed
Channel status:	byte 00 processed (*)
Subframe parity:	checked for even parity

Subframes A are read at the input. This is a safety measure, because the recorder processes emphasis and sampling frequency in stereo mode only.

(+) According to the standards AES-5 and ANSI S4-28, the accuracy of the sampling frequency shall be within ± 10 ppm.

Output with transformer coupling (serial no. 1071 up):

According to AES3-1985, ANSI S4.40-1985, IEC/CEI 958:1989)

Output voltage:	typ. 4V peak-to-peak across 110 Ω
Output impedance:	typ. 100 Ω, 100 Hz ... 6 MHz
Frequency accuracy:	see technical specifications
Output skew:	typ. 2.0 nsec.
Transition asymm.:	less than 10 nsec.
Rise and fall time:	typ. 60 nsec. (10 ... 90% amplitude)
Connector type:	XLR, pin 2 in-phase
Short circuit protection	
AC coupling	
Validity bit:	set to default value (logic zero)
User data:	set to default value (logic zero)
Channel status:	bytes 00 and 23 processed (*) bytes 01 to 22 set to logic zero
Subframe parity:	generated (even parity)

(*) content of byte 00:

bit 0:	0 = consumer, 1 = professional use (**)
bit 1:	0 = audio , 1 = non-audio use (***)
bit 2,3,4:	emphasis (see key EMPHASIS for more information)
consumer:	bit 3 (emphasis) is processed in override disable mode
bit 5:	0 = source sampl. frequency locked, 1 = unlocked (****)
bit 6,7:	sampling frequency (see key SAMPLING FREQUENCY)

(*) content of byte 23: CRC word for the preceding 23 bytes according to the standard

(**) bit 0 is set to logical one (1) at the output.
An error message "ILLEGAL DI FORMAT" will be displayed when bit 0 has not been received in logical one (1) state. The remaining bits of the control word will the not be considered any further (exception: bit 3, emphasis). The message can be suppressed with key no. 064 in the menu (IGNORE DI C WORD).

(***) bit 1 processing: at the input, bit 1 is not considered, enabling recording of non-audio material with full audio capabilities (possible CD-I applications, etc.). At the output, bit 1 is set to logical zero (0), indicating audio use in all cases.

(****) bit 5 processing: if logical 1 is read by the input, all analogaudio outputs are muted and an error message "DI UNLOCK" is displayed. At the digital output bit 5 is set to logical 1 if the recorder is in varispeed or in unlock mode (deviation more than 100 ppm from nominal sampling frequency).

Subrames A and B are transmitted at the output of the recorder and are identical in all cases.
The blocking structure of the recorder will exhibit a simple integer ratio to frames (phase lock). The recorder phaselocks to DI data. No varispeed is possible in phaselock mode. See chapter 1.6 for more information on blocking structure.
The transmission code is selfclocking. Cellclock is derived from data. It is not possible to use an external clock to read data fed to the input of the recorder.
Some notes on cable length: the two main frequencies of the AES/ EBU format are 32 and 64 times the sampling frequency (1.5 and 3 MHz at 48 kHz, fundamental frequencies). The electrical format is according to RS-422, permitting approximately 36 m at 48 kHz and 40 m cable length at 44.1 kHz with good microphone cable. The use of good cable is mandatory (Neutrik cable is recommended). Transformers at the in- and outputs also have proven to give superior results regarding transmission capabilities.

1.7.4 Time Code

Input with transformer coupling:

Longitudinal time code (LTC)

Max. input voltage:	20 V peak-to-peak
Input sensitivity:	0.2 V peak-to-peak
Input impedance:	more than 2 kΩ (standard biphase time code frequencies)
Connector type:	XLR, pin 2 in-phase
AC coupling	

Output with transformer coupling:

Serial output data, identical in format to the input data

Output voltage:	typ. 1.5 V peak-to-peak with board 1.861.771.00 (*)
Output voltage:	typ. 2.2 V peak-to-peak with board 1.861.770.00 (*)
Output volt. tol.:	± 0.1 V
Output impedance:	typ. 40 Ω, (standard biphase time code frequencies)
Connector type:	XLR, pin 2 in-phase
Last frame:	no repetition
Short circuit protection	
AC coupling	

(*) into open circuit

The time code output is aligned with data of the main channels (set appropriate frame rate in the menu), but not time base corrected. There will be a timing jitter relative to data due to the wow and flutter values.

1.7.5 Reference Time

Output with Transformer Coupling (Serial No. 1071 up):

Serial output data, format according to the DASH document (as on tape)

Sector rate:	500 Hz at 48 kHz sampling frequency
Output voltage:	typ. 3 V peak-to-peak across 500 Ω
Output impedance:	typ. 35 Ω, 100 Hz ... 6 MHz
Output skew:	typ. 2.0 nsec.
Connector type:	XLR, pin 2 in-phase

Short circuit protection
AC coupling

The time code output is time base corrected and precisely aligned with data in order to ease interfacing with editors and other devices requiring word synchronicity.

1.7.6 Composite Video / Composite Sync

Unsymmetrical Input:

Accepts 1/2-frame rates of all tv standards (PAL, SECAM, NTSC)

Max. input voltage:	3.5 V peak-to-peak
Input sensitivity:	0.25 V peak-to-peak
Input impedance:	75 Ω or typ. 100 kΩ, jumper selectable
Input coupling:	AC
Frequency accuracy:	50, 60/1.001, 60 Hz ± 100 ppm
Polarity:	positive/negative sync, jumper selectable
Connector type:	BNC female, isolated

Accepts any square wave. The blocking structure of the recorder will exhibit no relation to odd or even frames (frequency lock only).

1.7.7 Videoclock

Symmetrical Input:

Accepts 1/2-frame rates of all TV standards (PAL, SECAM, NTSC)

Waveform:	square wave
Max. input voltage:	± 12 V peak
Input sensitivity:	± 0.5 V peak
Input impedance:	more than 4 kΩ
Input coupling:	DC
Frequency accuracy:	50, 60/1.001, 60 Hz ± 100 ppm
Connector type:	DSub25 (External Clock connector)

The blocking structure of the recorder will exhibit no relation to odd or even frames (frequency lock only).

1.7.8 Wordclock/Sectorclock

Unsymmetrical Input (Wordclock Only):

According to RS-423 standard (or pseudo TTL, denoted with *)

Frequency:	according to internal crystal configuration
Waveform:	square wave
Max. input voltage:	± 12 V peak
Input sensitivity:	± 0.5 V peak (*)
Input impedance:	more than 2 kΩ or 75 Ω, jumper selectable
Input coupling:	AC
Data loading:	on trailing edge
Frequency accuracy:	sampling rate ± 100 ppm (***)
Connector type:	BNC female, isolated

The blocking structure of the recorder will exhibit a simple integer ratio to the wordclock (phase lock). No varispeed possible in phase lock.

Symmetrical Input (Wordclock Only):

According to RS-422 standard

Frequency:	according to internal crystal configuration
Waveform:	square wave
Max. input voltage:	± 12 V peak
Input sensitivity:	± 0.5 V peak
Input impedance:	more than 4 kΩ
Input coupling:	DC
Data loading:	on rising edge
Frequency accuracy:	sampling rate ± 100 ppm (***)
Connector type:	DSub25 (External Clock connector)

The blocking structure of the recorder will exhibit a simple integer ratio to the wordclock (phase lock). No varispeed possible in phase lock.

(***) According to the standards AES-5 and ANSI S4-28, the accuracy of the sampling frequency shall be within ± 10 ppm.

Unsymmetrical Output:

According to RS-423 standard or pseudo-TTL (denoted with *)

Sector rate:	500 Hz at 48 kHz sampling frequency (****)
Output voltage:	± 6 V peak into open circuit (*), jumper selectable on Timing + Test board 1.861.063/064/065
Output impedance:	typ. 35 Ω, 500 Hz ... 50 kHz
Frequency accuracy:	see technical specifications
Output skew:	typ. 2.0 nsec.
Connector type:	BNC female, isolated

Short circuit protection

Slew rate may be varied with capacitor on Timing + Test board

Symmetrical Output: According to RS-422 standard

Sector rate:	500 Hz at 48 kHz sampling frequency (****)
Output voltage:	typ. 6 V peak between outputs into open circuit
Output impedance:	typ. 35 Ω, 500 Hz ... 50 kHz
Frequency accuracy:	see technical specifications
Output skew:	typ. 2.0 nsec.
Connector type:	DSub25 (EXTERNAL CLOCK connector)

Short circuit protection

(****) frequency = (500 * fs)/48000
The sector rate may be non-continous (i.e. during splices)

1.7.9 Synchronizer Input

Waveform:	square wave
Max. input voltage:	+ 30 V peak
Input sensitivity:	+ 1 V peak
Recommended level:	TTL
Input impedance:	typ. 100 kΩ
Input coupling:	DC

The input is an unbalanced, protected hi-Z type (approx. 100 kΩ), feeding an HC14 schmitt-trigger. The synchronizer frequencies (SR- REFEXT) and their relationships to the sampling frequency, the crystal frequency, the tape speed and the division factors to obtain the SR-REFEXT signal from the crystal frequency are tabulated below:

SAMPLINGFR. (kHz)	X-TALFR. (MHz)	SR-REFEXT (kHz)	DIVISION FACTORS	TAPE SPEED (ips.)
48.0	27.6480	10.017391	2/6/230	15.0
46.0 (*)	---	9.60	---	14.3750 (**)
44.1	25.40160	9.2034782	2/6/230	13.78125
44.05594406	25.376224	9.194284	2/6/230	13.767482
32.0	18.4320	10.017391	2/4/230	10.0
30.666 (*)	---	9.60	---	9.58333 (***)

(*) virtual sampling frequency
(**) TSHI
(***) TSLO

SR-REFEXT: synchronizer input frequency

Note: from the table above it is obvious that the input frequency is 9.6 kHz only for the virtual sampling frequencies and tape speeds. There will be no problem with any synchronizer, because the recorder and the synchronizer form a feedback loop and the synchronizer produces an offset frequency in order to establish the nominal speed which is well within the range of any synchronizer. The control range is only minimally affected.

Due to possible instabilities there is no Reference Time readout as long as SYNC IN SYNCHRONIZER is selected. The last valid RT Control Word is frozen, meaning that sampling frequency, format version and auxiliary track format information is not updated during the chase phase.

The D820X can lock to a synchronizing source over a wide frequency range:
Capstan speed control of signal /SR-REFEXT/: 6 ... 13.5 kHz
Range of valid digitalaudio for /SR-REFEXT/: 6 ... 11.3 kHz

Caution: **out-of-range signals may cause permanent muting conditions!** Power-down may be necessary to establish normal operation.

Note: dBV.7 denotes absolute voltage level re 0.775 V.

1.8
Standard Calibration Data

Set-up data is transferred from ROM (where the default values are located) into RAM and to the hardware in the event that RAM data is lost. The choosen values ensure that the recorder can still be used despite this loss of data, albeit possibly with some degradation in performance. RAM data is not intended as a substitute for individual calibration (to compensate component and manufacturing tolerances).
Tape tension play, wind and edit values in the table below are shown in hexadecimal numbers. They will appear in the same form on the LC display. There is no direct conversion to tension in grams etc. because of the individual tolerances of the tape tension gauges. Note that it may be necessary to readjust the tape tension after RAM data failure since the default values only represent an approximation of the exact value.

Table 1

	key	power up	RAM init.
Panel:	Channel Control:		
	CH1, CH2, AUX, TC	SAFE*)/REPRO	SAFE*)/REPRO
	RT SYNC	OFF	OFF
Display:	TIME	ON (save times)	ON (time, lap: 0)
	PEAK RESET	RESET	RESET
	CAL GAIN/UNCAL	CAL	CAL (cal; uncal: = cal
	HEAD ROOM GAIN	OFF (cal)	OFF (cal)
Monitor:	INPUT/TAPE	TAPE	TAPE
	CH1, CH2, CUE1, CUE2	LS	CUE1, CUE2
Softkeys:	MASTER SAFE	LS	OFF
	44.1	LS	HIGH
	INPUT DIGITAL	LS	ANALOG
	EMPHASIS	LS	OFF
	DATA/CUE	LS	OFF
	REHEARSE	OFF	OFF
	REMOTE	LS	OFF
	FADER START	LS	OFF
	EXT SYNC	LS	OFF
	VARISPEED	OFF	OFF
	AUTO INPUT	LS	OFF
	AUTO EDIT	LS	OFF
	SET VARISPEED	OFF	OFF
	RT SYNC	OFF	OFF
	TC SAFE	SAFE	SAFE

Note: *) panel version only (D820X-2/2PPM)
LS = last setting

Table 2

key	power up	RAM init.
CLIPPPING LEVEL INPUT	LS	15dBm/15dBm
CLIPPPING LEVEL OUTPUT	LS	15dBm/15dBm
DIGITAL GAIN INPUT	LS	0dB/0dB
DIGITAL GAIN OUTPUT	LS	0dB/0dB
CUE LEVEL	LS	15dBm/15dBm
RECORD CURRENT A	LS	95mA
RECORD CURRENT B	LS	95mA
REFERENCE EQ TABLE	LS	not selected
STOP ADAPTATION	LS	not selected
PAR BACKUP RS232	↓ ↑	↓ ↑
PARAM BACKUP ON TAPE	↓ ↑	↓ ↑
HUB DIAMETER LEFT SET	LS	NAB 118
HUB DIAMETER RIGHT SET	LS	NAB 118
SET LIBR WIND SPEED	LS	2.5 m/s
SET MAX WIND SPEED	LS	10 m/s
SET ROLLBACK TIME	LS	15 sec
TAPE TENSION PLAY (left/right)	LS	85/85
TAPE TENSION WIND	LS	85
TAPE TENSION EDIT	LS	89
SET ES BUS ADDRESS	LS	MSB:82/LSB:80
BIN RS232/422 FORMAT	LS	8Bit, 1Stop
ASCII RS232 BAUD RATE	LS	9600
ASCII RS232 MODE	LS	no echo
SET LED STOP-FORMAT	LS	1/10
SET LED MOVE-FORMAT	LS	1/10
SET LEADING ZEROS	LS	0.ss

Note: LS = last setting
↓ = arrow down
↑ = arrow up

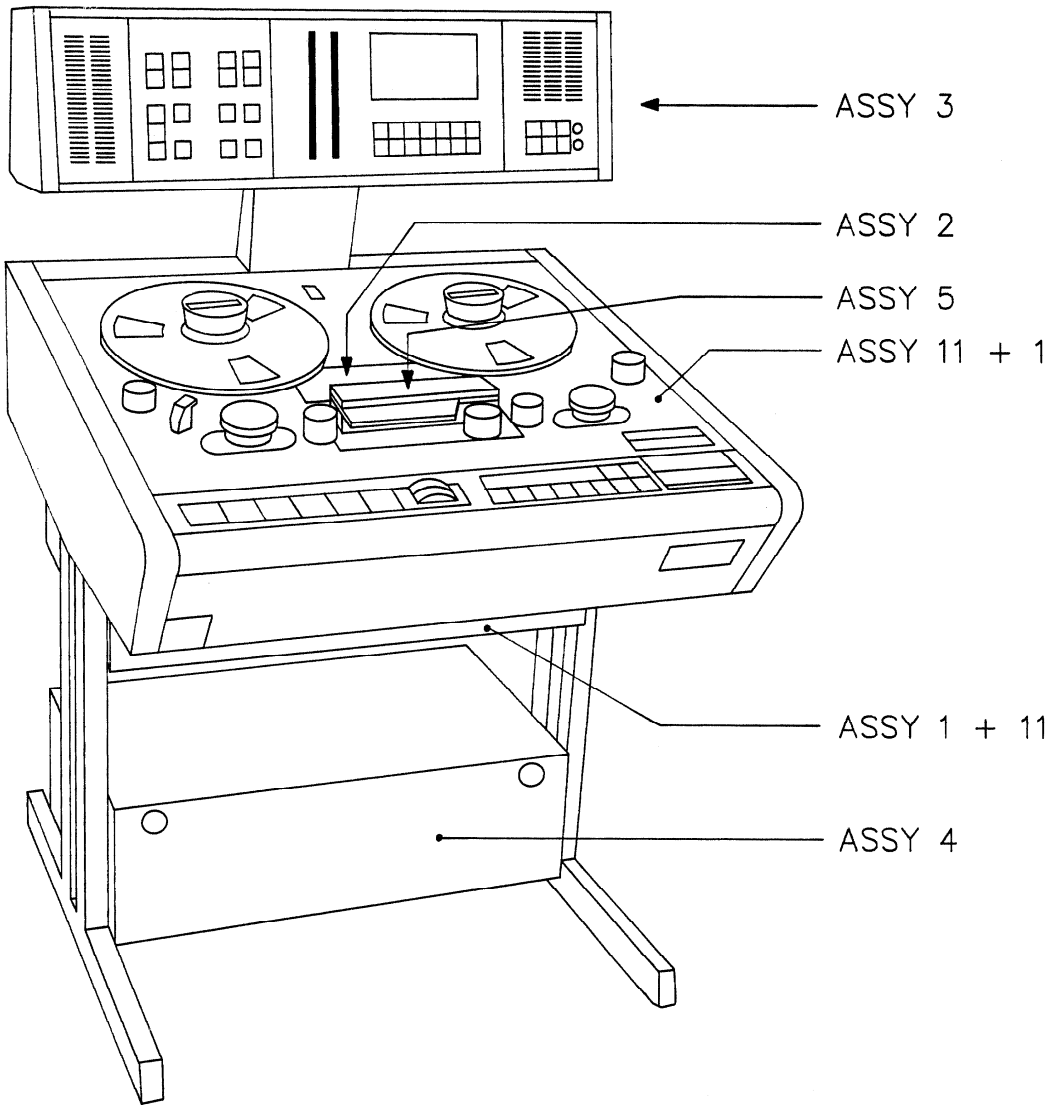
Table 3

	function	pwr-up	RAM init.	status field LED	assigned local	assigned serial rem	assigned parall rem
KEYS/MODE	001 CLIP LEVEL 4dbm Y/N	LS	N				
	002 CLIP LEVEL 6dbm Y/N	LS	N				
	003 CLIP LEVEL 8dbm Y/N	LS	N				
	004 CLIP LEVEL 10dbm Y/N	LS	N				
	005 CLIP LEVEL 15dbm Y/N	LS	N				
	006 CLIP LEVEL 20dbm Y/N	LS	Y				
	007 CLIP LEVEL 24dbm Y/N	LS	N				
	008 DIGITAL GAIN 0db Y/N	LS	N				
	010 INPUT Y/N	N	N		PANEL		
	011 REPRO Y/N	Y	Y		PANEL		
	014 AUTOINPUT A: Y/N	LS	N				
	015 AUTOINPUT B: Y/N	LS	N		L27/-		
	016 AUTOMUTE: ON/OFF	LS	OFF				
	017 AUTOEDIT: ON/OFF	LS	OFF		L26/-		
	018 INPUT: DIGITAL/ANALOG	LS	ANALOG	yellow	L37		
	019 EMPHASIS: ON/OFF	LS	OFF	yellow	L34		
	020 SAMPLING RATE: LO/HI	LS	HI		L33		
	021 SAMPLING RATE HI: Y/N	LS	Y	yellow			
	022 SAMPLING RATE LO: Y/N	LS	N	yellow			
	023 SYNCHRONIZER ON/OFF	LS	ON				
	025 CH CONTR: PAR/INDIV	LS	INDIV				
	030 CHANNEL1: SAFE/READY	SAFE*	SAFE		PANEL		
	033 CHANNEL2: SAFE/READY	SAFE*	SAFE		PANEL		
	036 TIMECODE: SAFE/READY	SAFE	SAFE	green	P/L27		
	039 RT SYNC: ON/OFF	OFF	OFF	yellow	P/L26		
	042 AUX 3: SAFE/READY	SAFE	SAFE		PANEL		
	043 MASTER SAFE: ON/OFF	LS	OFF	green	L36		
	044 ASSIGN AUX3: DATA/CUE	LS	CUE	yellow			
	045 AUX3+4: MANUAL/AUTO	LS	AUTO				
	046 CUE: UNMODULATED/AUTO	LS	AUTO				
	047 CUE: MODULATED/AUTO	LS	AUTO				
	048 HIGH PASS FIL: ON/OFF	LS	OFF				
	049 QUALITY DISP: ON/OFF	LS	ON				
	050 LEVEL DISP: NORM/INPT	LS	NORM				
	051 SYNC IN: EXT/INT	LS	INT	red	L35		
	052 SYNC IN: BAL/UNBAL	LS	UNBAL				
	053 SYNC IN WORD CLK: Y/N	LS	Y				
	054 SYNC IN DIG INPT: Y/N	LS	N				
	055 SYNC IN VID EBU: Y/N	LS	N				
	056 SYNC IN NTSC B/W: Y/N	LS	N				
	057 SYNC IN NTSC COL: Y/N	LS	N				
	058 SYNC IN SYNCHR: Y/N	LS	N				
	058 SYNC IN SYNCHR: Y/N	LS	N				
	059 SYNCOUT SECT CLK: Y/N	LS	N				
	060 SYNCOUT WORD CLK: Y/N	LS	Y				
	064 IGNORE DI C WORD: Y/N	LS	N				
	065 MASTERING ON: Y/N	LS	N				
	070 TEST ON/OFF	OFF	OFF				
KEYS ONLY	101 REHEARSE	OFF	OFF	yellow			
KEYS/MODE	201 TAPE GUARD A NO/RED	LS	RED				
	202 TAPE GUARD B NO/STOP	LS	STOP				
	210 VARISPEED % Y/N	LS	Y				
	211 VARISPEED HT Y/N	LS	N				
	212 VARISPEED IPS Y/N	LS	N				
	213 VARISPEED %/IPS/HT	LS	%				
	214 VS INO ENHANCED Y/N	LS	N				
	220 FADER START A Y/N	LS	N	yellow			R 74
	221 FADER START B Y/N	LS	Y	yellow	L23	R 10	R 74
	222 FADER START C Y/N	LS	N	yellow			R 74
	223 FADER START D Y/N	LS	N	yellow			R 74

KEYS ONLY	301 REWIND	OFF	OFF		L07	R 06	R 67
	302 FORWARD	OFF	OFF		L06	R 05	R 66
	303 LIBRARY WIND SPEED	OFF	OFF		L13		
	304 PLAY	OFF	OFF		L05	R 04	R 65
	306 STOP	OFF	OFF		L04	R 03	R 64
	307 RECORD A	OFF	OFF		L03	R 02	R 63
	307 RECORD B	OFF	OFF				R 63
	309 EDIT	OFF	OFF		L02		
	310 CUT	OFF	OFF		L12		
	311 TRANSFER	OFF	OFF		L17	R 26	
	312 HOLD	OFF	OFF				
	313 LOCATOR 1	OFF	OFF		L16	R 25	
	314 LOCATOR 2	OFF	OFF			R 24	
	315 LOCATOR 3	OFF	OFF			R 23	
	316 LOCATOR 4	OFF	OFF				
	317 LOCATOR 5	OFF	OFF				
	318 ZERO LOCATOR	OFF	OFF		L15	R 22	R 70
	319 LOC START STOP	OFF	OFF				R 75
	320 LOC START PLAY	OFF	OFF		L14	R 21	R 75
	321 LOC START REC	OFF	OFF		L14	R 21	R 75
	322 ROLLBACK STOP	OFF	OFF				
	323 ROLLBACK PLAY	OFF	OFF			R 20	
	324 ROLLBACK REC	OFF	OFF				
	327 TAPE DUMP A	OFF	ON		L11		
	328 TAPE DUMP B	OFF	OFF				
	329 TAPE DUMP C	OFF	OFF				
	330 TAPE DUMP D	OFF	OFF				
	332 LIFTER	OFF	OFF				R 73
	334 START/STOP	START	START				
	335 RESET TIMER	OFF	OFF		L41	R 41	R 71
	336 SET TIMER	OFF	OFF				
	337 SET ADDRESS	OFF	OFF				
	338 SET VARISPEED	OFF	OFF		L24		
	339 VARISPEED ON/OFF	OFF	OFF	red	L25		
	345 REMOTE A	OFF	OFF	yellow			
	346 REMOTE B	OFF	OFF	yellow			
	347 SHUTTLE BAR	OFF	OFF		L10	R 00	
	355 TIME DISPLAY	ON	ON				
	356 WATCH DISPLAY	OFF	OFF				
	357 RT DISPLAY	OFF	OFF				
	358 TIMECODE DISPLAY	TIME	TIME				
	359 TIME/WATCH DISPLAY	TIME	TIME				
	360 TIME/WATCH/RT/TC DIS	TIME	TIME		L40	R 40	
	361 UNLOAD	OFF	OFF		L10		
	362 NO FUNCTION	OFF	OFF				
KEYS/MODE	401 25 F/SEC: Y/N	LS	Y				
	402 29.97 F/SEC: Y/N	LS	N				
	403 30 F/SEC: Y/N	LS	N				
	404 25/29.97/30 F/SEC	LS	25				
	405 25/29.97 F/SEC	LS	25				
	406 29.97/30 F/SEC	LS	N				
	407 DISPLAY CODE: Y/N	LS	Y				
	408 DISPLAY USER BITS: Y/N	LS	N				
	409 DISP. UNASS. BITS: Y/N	LS	N				
	410 DISPLAY USER/CODE	LS	CODE				
	411 CODE/USER/UNASSIGNED	LS	CODE				
	415 TC: UNMODULATED/AUTO	LS	AUTO				
	416 TC: MODULATED/AUTO	LS	AUTO				
	425 TC DELAY: OFF/AUTO	LS	AUTO				
	426 TC DELAY: ON/AUTO	LS	AUTO				
KEYS ONLY	501 FOR FUTURE USE ONLY	OFF	OFF				

Note: LS = last setting

1.9
Location and Designation of Main Parts



1.10 Maintenance Hints for the Service Personnel

1.10.1 General

The following method is used for defining the IC position numbers:
With the component side of the PCB facing the viewer and with the edge connector on the right-hand side, an imaginary coordinate network is overlayed on the component side. Each square takes the space occupied by a DIL-16 IC. For a European standard board (100 mm x 160 mm) there is space for 48 ICs, corresponding to six columns and eight rows. The reference point for the IC is the IC corner located nearest to coordinate 1/1.

The column is in the tens position, the row in the units position. Together they give the IC position number.

Example: IC 48
- Row 8
- Column 4

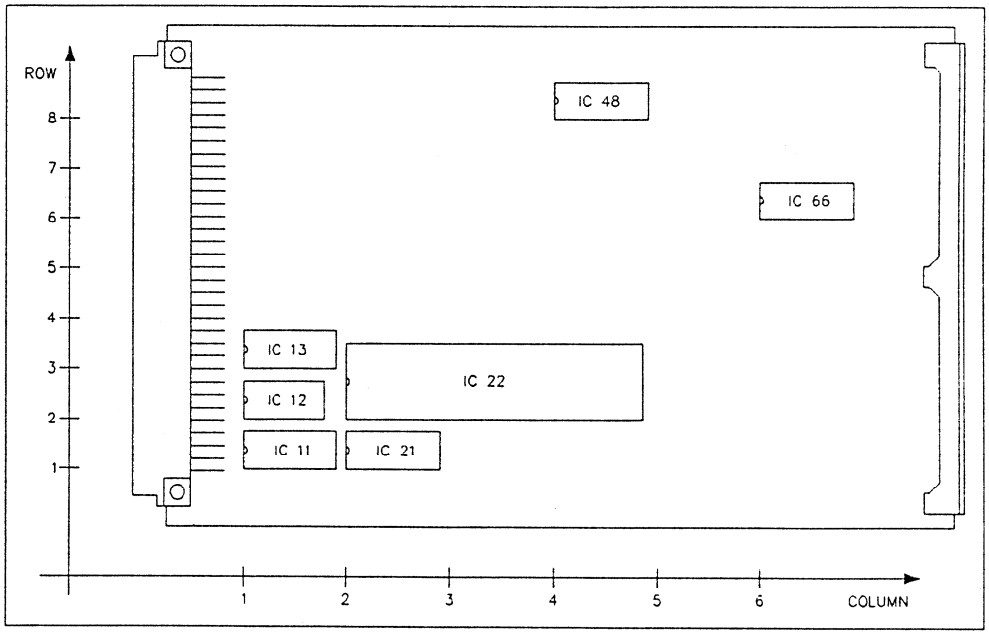


Fig. 1.10.1

Exeption: Boards in the PCM-Box. The columns carry numbers 100*n, with n = positive integer.

1.10.2 Abbreviations

A	assembly
ANT	antenna
B	bulb
BA	battery, accumulator
BR	optocoupler (bulb --> LDR)
C	capacitor
D	diode, DIAC
DL	LED
DLQ	optocoupler (LED --> phototransistor)
DLR	optocoupler (LED --> LDR)
DLZ	LED-array, 7 segment display
DP	photodiode
DZ	rectifier
E	electronic part
EF	headphones
F	fuse
FL	filter
H	head (sound-, erase-)
HC	hybrid circuit (thick/thin film)
HE	hall element
IC	integrated circuit
J	jack (femal)
JS	jumper
K	relay, contactor
L	inductor
LS	loudspeaker
M	motor
ME	meter
MIC	microphone
MP	mechanical part
P	plug (male)
PU	pick up
Q	transistor, FET, thyristor, TRIAC
QP	phototransistor
QPZ	phototransistor array
R	resistor
RP	light depending resistor (LDR)
RT	temperature sensitive resistor
RZ	resistor array
S	switch
T	transformer
TL	delay line
TP	test point
W	wire, stranded wire
X	socket, holder
XB	lamp socket
XF	fuse holder
XIC	IC socket
Y	quartz, piezoelectric element
Z	network, array

These abbreviations may be combined (max. 3 characters)

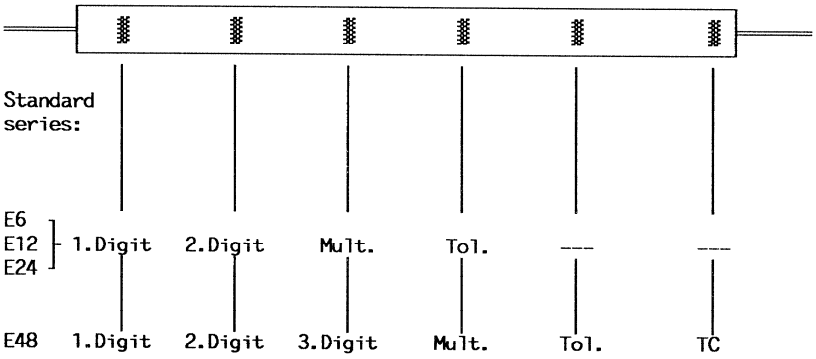
1.10.3 Powers of Ten

Name	Abbreviation	Value
Tera-	T	10**12
Giga-	G	10**9
Mega-	M	10**6
Kilo-	k	10**3
Milli-	m	10**-3
Mikro-	µ	10**-6
Nano-	n (mµ#)	10**-9
Pico-	p (µµ#)	10**-12
Femto-	f	10**-15

frequently used in the United States

1.10.4 Code Letters and Colors

Resistor



Color	Digit	Multiplier	Tolerance	Temp.-coefficient
gold	-	0,01	5 %	-
silver	-	0,1	10 %	-
black	0	1	-	-
brown	1	10	1 %	100 * 10 ** -6 / K
red	2	100	2 %	50 * 10 ** -6 / K ##
orange	3	1 k	-	15 * 10 ** -6 / K
yellow	4	10 k	-	25 * 10 ** -6 / K
green	5	100 k	0,5 %	-
blue	6	1 M	0,25 %	-
violet	7	10 M	0,1 %	-
grey	8	-	-	-
white	9	-	-	-

either no mark for temperature coefficient, or red

Capacitors

The tolerance category is sometimes specified by a letter after the rated capacitance.

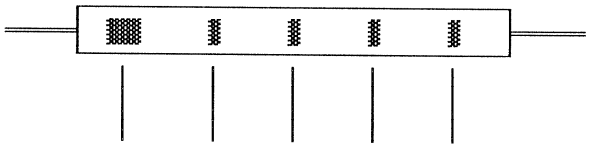
D = 0,5%
F = 1%
G = 2%
J = 5%
K = 10%
M = 20%

Molded RF Coils

A wide silver-colored ring and 4 thin, differently colored rings identify molded RF coils. The wide silver ring indicates the start of the counting direction. The second, third, and fourth ring indicate the inductance in micro Henry (µH), where two of the three rings represent the numeric value, the third one either a multiplier or the decimal point. In the latter case it has a golden color. The fifth ring indicates the tolerance in precent (±).

Color	Digit	Multiplier	Tolerance
black	0	1	-
brown	1	10	1 %
red	2	100	2 %
orange	3	10**3	-
yellow	4	10**4	-
green	5	10**5	0,5 %
blue	6	10**6	-
violet	7	10**7	-
grey	8	10**8	-
white	9	10**9	-
gold	,	-	5 %
silver	-	-	10 %
any (nat).	-	-	20 %

Examples:



silver gold* brown green silver = 0,15 µH 10%

silver red gold* violet --- = 2,7 µH 20%

silver grey red brown** gold = 820 µH 5%

* Dezimal point
** Multiplier

Inductors, Transformers on Ferrit Cores

Inductors and transformers on ferrite cores are marked with three colored dots (for color codes, refer to the table in the section "Resistors", the two left-hand columns). These dots represent the last three digits of the STUDER standard number, the largest of them identifying the start. The first gigits of the standard number (1.022.---) are always the same.

Examples:

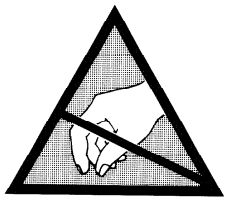
Driver Transformer, 150 kHz.
Standard number: 1.022.211
Color code: red (large dot), brown, brown

Terminal 1 of the winding form is usually identified by a lobe; if not the winding form features a yellow dot near terminal No. 1.

1.10.5
Components Sensitive to Electrostatic Charges

MOS (Metal oxide semiconductor) components are extremely sensitive to static charges. Please observe therefore the following regulations:

- Components sensitive to static charges are stored and shipped in protective packages. On the packages you find the subsequent symbol:



- Avoid any contact of connector pins with foam packages and -foils made styrofoam or similar chargeable package material.
- Don't touch the connector pins unless your wrist is grounded with a conducting wristlet.
- Use a grounded conducting mat when working with sensitive components.
- Never plug or unplug PCBs containing sensitive components when the equipment is switched on. Before plugging or unplugging PCBs, the equipment has to be switched off for fife seconds at least!

Table of Contents Section 2: Startup Procedures

2 Startup Procedures

2.1 Unpacking and Testing

The D820X tape recorder is delivered in special packing material which protects it from damage in transit. Care should be exercised when unpacking the recorder so that the equipment surfaces will not become marred.
Compare the content with the packing slip to ensure that the equipment is complete. Save the original packing material since it provides the best protection of the recorder for subsequent shipment.
Examine the complete content for possible transit damage. The forwarding company and the nearest STUDER dealer should be notified immediately in the event of damage.

2.2 Place of Installation

The recorder should be installed in a well ventilated location that is as dust-free as possible. The recorder specifications are guaranteed for ambient temperatures ranging from 0 to 40 centigrade. The relative humidity (non condensing) should range between 20 and 90%.
Install the recorder in such a place that there is sufficient space for unrestricted ventilation. Particularly when a recorder is installed in a recess, localization of heat can occur. The air circulation zone should not be used as a storage area for manuals, tapes, etc.
The recorder must not be placed in close proximity to strong electromagnetic (EMI) fields. General sources of such interference are: strong load fluctuations on adjacent power lines, high-power transformers, elevator motors, as well as nearby radio and television transmitters.
It also should not be placed in close proximity to strong radio frequency (RFI) fields as produced by terminals, TV screens, computer equipment, etc. Check the LED display on the board ADAPTIVE RUN PROCESSOR 1.861.760 in the PCM box for a non-flickering display.

The back of the recorder should remain accessible for maintenance purposes. If the recorder is installed in a recess, sufficient clearance for shifting the recorder should remain even after the cables are attached.

2.2.1 Operating Positions

The equipment specifications are guaranteed for any operating position between horizontal or ± 7.5 and ± 15 degree inclination.

Caution! During fast wind operations the console tilting mechanism must not be actuated - tape, reels, reel adaptors, and tape transport cover may be seriously damaged as a result of the high gyro forces!

2.3 Installing the Recorder

2.3.1 Installation of Console

The recorder is shipped in disassembled condition. First the console side panels with mounted rollers or floor slides are to be screwed (Allen key 5 mm) to the traverse (or the rack base) after which the tape deck can be placed on top and fastened (Allen key 6 mm). Secure the wooden side panels with 4 screws each (Allen key 4 mm).

2.3.2 Installation of PCM Box

The rack containing the PCM electronics at the bottom of the console is connected to the transport by means of three DSub25 connectors, labeled BOX-RACK 1...3. Insert the connectors at their appropriate place (the ribbon cables carry a label) and fasten the screws at each side of the connectors. Insert the power cord from the box into the transport mains connector. The external mains voltage is to be applied to the power supply located in the box. Refer to chapter 2.4.2 for mains voltage selectors and to chapter 3.2.1.4 for power supply distribution.

2.4
Interfacing, Remotes

2.4.1
Overview of Connectors

2.4.1.2
AC Power, Voltage Selector

2.4.1.3
XLR Connectors

2.4.1.4
External Clock Connector

Pin	Signal name	Description
01	SYWDIOUT	Sectorclk or Wordclk Out Balanced *
02	WDIIN	Wordclock Input Balanced *
03	VIDICLK	Videoclock Input Balanced *
04	NC	
05	NC	
06	RTIOUT	Reference time output *
07	RES31	Spare interconnection to RT/TC CODEC
08	NC	
09	NC	
10	NC	
11	NC	
12	+0V-	Digital ground
13	+0V-	Digital ground
14	SYWDOUT	Sectorclk or Wordclk Out Balanced
15	WDIN	Wordclock Input Balanced
16	VIDCLK	Videoclock Input Balanced
17	NC	
18	NC	
19	RTOUT	Reference time output
20	RES32	Spare interconnection to RT/TC CODEC
21	NC	
22	NC	
23	NC	
24	NC	
25	+0V-	Digital ground

NC = not connected
* = inverse polarity

2.4.1.5
Test Connector

Pin	Signal name	Description
01	NC	
02	TSTSIFRD	Terminal/PC Interconnection rcv
03	TSTSIFTD	Terminal/PC Interconnection xmt
04	NC	
05	NC	
06	NC	
07	+0V-	Ground
08	NC	
09	NC	
10	NC	
11	NC	
12	NC	
13	NC	
14	NC	
15	NC	
16	NC	
17	NC	
18	NC	
19	NC	
20	NC	
21	NC	
22	NC	
23	NC	
24	NC	
25	NC	

NC = not connected

Supported terminal drivers

1 ASCII	simple ASCII
2 ESPRIT	esprit terminals by Hazeltine
3 HP	Hewlett-Packard terminals
4 TVI905	Televideo 905 terminal
5 ANSI	several manufacturers (e.g. IBM-PC)

2.4.1.6
Clock Connectors

2.4.1.7
Remote Control Connectors

Connector PARALLEL REMOTE CONTROL

A 25-way connector (female, type D) permits connection of a parallel remote control with the following features:

- Remote control of tape transport functions with acknowledgment (◄, ►, PLAY, STOP, REC)
- RESET TIMER (resetting of the tape counter)
- ZERO LOC (automatic searching of the tape counter address 0.00.00.0)
- LOC START (automatic searching of the tape counter address at which the last PLAY command was entered), with LED
- BACKSPACE (programmable rollback and play function)
- FADER (enabling of fader start circuit), with LED

Connector set	Part No.	20.020.303.16
Connector housing, 25 pins	Part No.	54.13.7022
Connector, 25 pins, coded	Part No.	10.217.001.06

Pin assignment of the PARALLEL REMOTE CONTROL connector:

Pin	Signal name		Description
01	+0.0		ground
02	BR-REW	*	lamp REWIND achieved
03	BR-FORW	*	lamp FORWARD achieved
04	BR-VRSPD	*	lamp VARISPEED achieved (if active, alternating LOW and HIGH)
05	SR-VRSPD	+	switch for VARISPEED command
06	SR-FADRY	+	switch for FADER START READY command
07	BR-LOCST	*	lamp LOC START achieved
08	BR-FADRY	*	lamp FADER START READY achieved
09	BR-REC	*	lamp RECORD achieved
10	SR-RESET	+	switch for RESET TIMER command
11	FAD1		input FADER START command, line A
12	FAD2		input FADER START command, line B (FADER START active if 5 to 24 V AC or DC between pins 11 and 12)
13	IR-REFEX		input for ext. speed reference (see interfacing specifications, par. 1.7.9)
14	SR-OLOC	+	switch for ZERO LOC command
15	BR-PLAY	*	lamp PLAY achieved
16	BR-STOP	*	lamp STOP achieved
17	SR-LIFT	+	switch for LIFTER command
18	SR-LOCST	+	switch for LOC START command
19	SR-REC	+	switch for RECORD command
20	SR-REW	+	switch for REWIND command
21	SR-FORW	+	switch for FORWARD command
22	SR-PLAY	+	switch for PLAY command
23	SR-STOP	+	switch for STOP command
24	KEY		coding
25	+24.0		supply +24 V (300 mA max.)

* Open collector output, active LOW. No internal pull-up resistor, max. HIGH level = 30 V. Sink current 200 mA max., internal current limit resistor 22 Ohm.

\+ Switch input, LOW level activates command. Internal pull-up resistor 4.7 kOhm connected to +24 V, max. HIGH input level = 30 V. Logic levels: LOW: 0 V to 4 V; HIGH: 7.5 V to 30 V.

Caution! If light bulbs are used as acknowledgement lamps, their inrush current must not exceed 0.3 A.

Connector EXTERNAL SYNCHRONIZER

A 25-way connector (female, type D) is available for connecting an external synchronizer.

Connector set	Part No.	20.020.303.15
Connector housing, 25 pins	Part No.	54.13.7022
Connector, 25 pins, coded	Part No.	10.217.001.05

Pin assignment of the EXTERNAL SYNCHRONIZER connector:

Pin	Signal name		Description
01	+0.0		ground
02	BR-REW	*	lamp REWIND achieved
03	BR-FORW	*	lamp FORWARD achieved
04	BR-VRSPD	*	lamp VARISPEED achieved (if active, alternating LOW and HIGH)
05	SR-VRSPD	+	switch for VARISPEED command
06	SR-REHSL	+	switch for REHEARSAL command
07	OR-MVCLK	*	output for TAPE MOVE CLOCK signal (512 pulses/second, duty cycle=50 %, for 48 kHz sampling frequency)
08	KEY		coding
09	BR-REC	*	lamp RECORD achieved
10	OR-MVDIR	*	output for signal TAPE MOVE DIRECTION (rewind = LOW, forward = HIGH)
11	OR-CMCLK	*	output f. signal CAPST. M. MOVE CLOCK (2400 pulses/second for 48 kHz sampling frequency)
12	OR-SYENB		output for signal SYNCHRONIZER ENABLE (LOW if tape loaded & recorder ready; HIGH if tape not tensioned)
13	IR-REFEX		input for ext. speed reference (see interfacing specifications, par. 1.7.9)
14	+0.0		ground
15	BR-PLAY	*	lamp PLAY achieved
16	BR-STOP	*	lamp STOP achieved
17	SR-LIFT	+	switch for LIFTER command
18	SR-MUTE	+	switch for MUTE command (TC channel not affected)
19	SR-REC	+	switch for RECORD command
20	SR-REW	+	switch for REWIND command
21	SR-FORW	+	switch for FORWARD command
22	SR-PLAY	+	switch for PLAY command
23	SR-STOP	+	switch for STOP command
24	KEY		coding
25	+24.0		supply +24 V (300 mA max.)

* Open collector output, active LOW. No internal pull-up resistor, max. HIGH level = 30 V. Sink current 200 mA max., internal current limiting resistor 22 Ohm.

\+ Switch input, LOW level activates command. Internal pull-up resistor 4.7 kOhm connected to +24 V, max. HIGH input level = 30 V. Logic levels: LOW: 0 V to 4 V; HIGH: 7.5 V to 30 V.

Connector for RS-232 INTERFACE (ASCII or binary protocol), SMPTE/EBU BUS (ES-BUS), and DATA SAVE on tape or with personal computer

With option 1.810.751 Serial Remote Controller

These 9-way connectors (female, type D) permit connection of either a terminal or a computer with RS-232 interface (ASCII protocol) for control/display applications (see par. 2.10.5 below) or for back-up purposes, or a tape recorder for saving the audio parameters (streamer mode), or the STUDER Serial Controller 1.861.058 (see below). The streamer mode application uses the STUDER bus. Its pin assignment is described in the table "data save on tape".

The 9-pin connector (female, type D) permits connection of a serial remote control with the following standard features (the keys are reprogrammable):

- Remote control of tape transport functions with acknowledgment (◄, ►, PLAY, STOP, REC)
- SHUTTLE and SHUTTLE BAR
- RESET TIMER (resetting of the tape counter)
- TIME (displays all 4 time modes supported by the D820X)
- TRANS (for transfering time displays into locator memories)
- LOC 1...3 (3 locator memories, assignable to different functions)
- ZERO LOC (automatic searching of the tape counter address 0.00.00.0)
- LOC START (automatic searching of the tape counter address at which the last PLAY command was entered)
- ROLLBACK (programmable rollback)
- FADER (enabling of fader start circuit)

The keys of the serial remote control can be programmed by the user as desired. All functions available on the local keyboard can be operated with the remote controls. The functions programmed for the serial remote control do not necessarily have to be the same as those on the local keyboard.

Cabinet Part No. 1.861.058.00
Module Part No. 1.861.059.00
Counter Part No. 1.861.060.00

With option 1.820.751 Serial Remote Controller

These 9-pin connectors (female, type D) permit connection of a terminal with RS-232 interface (binary protocol) or the SMPTE/EBU (ES-) bus (RS-422) (option 1.820.751).

Connector set part No. 20.020.303.07

Pin assignment of the RS-232 or DATA SAVE connector (with option 1.810.751)

RS232/DSub9		
Pin	Signal name	Description
01	SHIELD/FRMGND	shield or screen
02	TRANSA/SNDATA	transmitted data
03	---	not to be connected
04	---	not to be connected
05	---	not to be connected
06	---	not to be connected
07	---	not to be connected
08	RECEIVA/RCVDATA	received data
09	SHIELD/FRMGND	shield or screen

The pin assignment described above is valid for the RS-232 ASCII protocol as well as the binary protocol, but then with option 1.820.751.

DATA SAVE ON TAPE/DSub9		
Pin	Signal name	Description
01	SHIELD/FRMGND	shield or screen
02	---	not to be connected
03	---	not to be connected
04	RECEIVCM/STUBUS1	in-/output (+)
05	---	not to be connected
06	TRANSCM/STUBUS2	in-/output (-)
07	---	not to be connected
08	---	not to be connected
09	SHIELD/FRMGND	shield or screen

The polarities of the in- and outputs are of no concern (biphase code)

Pin assignment of the RS-232 (binary protocol) or ES-BUS connector (with option 1.820.751)

ES-BUS/DSub9		
Pin	Signal name	Description
01	FG (*)	shield or screen
02	TA	transmitted data (-)
03	RB	received data (+)
04	RC	shield or screen
05	SPARE	not connected
06	TC	shield or screen
07	TB	transmitted data (+)
08	RA	received data (-)
09	FG (GND) (*)	shield or screen

* jumper selectable

Connector AUTOLOCATOR/REMOTE TIMER

The 9-pin connector (female, type D) permits connection of a serial remote control, of a remote counter, or an autolocator.

Pin assignment of the AUTOLOCATOR/REMOTE TIMER connector:

pin	signal name
01	SHIELD
02	N.C.
03	TR-A
04	KEY
05	+0.0
06	N.C.
07	TR-B
08	SIG.GND
09	+REMSUP

Supply voltage range of +REMSUP (worst case) = 35...60 VDC.

2.4.1.8
Display Panel Connector

Pin	Signal name	Description
01	DPCBCLK	Sysbus clock
02	DPCBAD	Sysbus address
03	DPCBDAT	Sysbus data
04	NC	
05	+0.0	Ground
06	+0.0	Ground
07	+0.0	Ground
08	+0.0	Ground
09	+0.0	Ground
10	+0.0	Ground
11	+0.0	Ground
12	+0.0	Ground
13	+0.0	Ground
14	DPCBICLK	Sysbus clock inverse
15	DPCBIAD	Sysbus address inverse
16	DPCBIDAT	Sysbus data inverse
17	NC	
18	NC	
19	+20PC	+20V
20	+20PC	+20V
21	+20PC	+20V
22	+20PC	+20V
23	+20PC	+20V
24	+20PC	+20V
25	+20PC	+20V

NC = not connected

2.4.1.9
Headphone Connector

2.5 Operating Instructions

2.5.1 Standard Key Assignment

2.5.1.1 D820X-2

2.5.1.2
D820X-2PPM

2.5.2 Power Switch

Caution! Before switching on the recorder for the first time, check that the setting of the AC voltage selector on the back of the recorder and on the power supply of the PCM box located beneath the transport matches the local line voltage. If the setting of the AC voltage selector is changed, check also the rating of the power fuse. For conversion to 100 V mains voltage, detailed instructions are available from your STUDER representative.

The power switch is located at the top edge of the tape transport cover. The switch handle must be pushed downward for this purpose. To switch the recorder off, push the switch handle upward.

The last operating state is automatically reestablished and indicated after the power is switched on (refer to par. 1.8: standard calibration data).

Exceptions: the recorder always enters STOP mode (the STOP button flashes if no tape is mounted or if the tape is mounted loosely). Recorders equipped with a SAFE/READY switch are switched to SAFE.

When the recorder is switched on, the microprocessor automatically tests the main functions; any error is indicated on the service display.

2.5.3 Pilot Lamps

The D820X features two lines of 8 colored LED pilot lamps on top of the secondary keyboard. They are illuminated when the corresponding function as indicated on the panel is achieved. The sampling rate indication is only illuminated when frequency and/or phase lock with the external source has been established.

Par. 2.5.27 contains additional information.

2.5.4
Mounting the Tape, Reel Hubs

Adapters for three-pronged (cine) reels and for DIN hubs are engaged in the spindle mounting; adapters for NAB reels or hubs are inserted in the spindle mounting and secured by pressing on the round button in the center of the adapter. All adapters can be released by lightly pressing against the rim of the spindle.
NAB reel: Mount NAB adapter. **Lock the adapters by pressing the round button in the center!** Self-supporting pancakes with NAB adapters are not recommended.

Three-pronged reel with flange: (DIN 45514, 45517) Mount adapter for three-pronged reels. Mount reels on the spindles. Pull out the three-pronged guide and lock it by rotating it 60 degrees.

Threading the tape

Thread the tape as shown in the illustration. The leading end of the tape is placed on the empty reel and secured with a few counterclockwise rotations. As soon as the tape is tensioned, the tape transport starts up and the STOP key flashes. When one of the tape command keys is pressed, the tape tension circuit is enabled and the D820X is ready for operation.
Set the absolute and/or relative tape counter and/or reference time to zero by pressing the RESET TIMER key after setting the TIME display key to show the appropriate time.

2.5.5 Tape Unloading

The unload key permits threading and removal of tapes without excessively touching it. This is important especially for digital recorders. Digital tapes should exhibit no fingerprints at all (distance losses). The function is equivalent to the tape out mode detected by the light barrier. It is a momentary function and is active as long as the key is pressed.
UNLOAD can be activated when either STOP, or EDIT, or tape out is achieved. The LED is illuminated as long as the key is pressed. The rollers in front of the headblock move out or in depending on the state of the recorder.
When UNLOAD has been activated, or a new tape has been loaded, the recorder looses its parameters for radius and reel inertia. The start-up time is then elongated. Winding the tape will remove this effect. Watch the tape tension guidances for a sudden change in position. The recorder has then adjusted to the new inertia conditions.

2.5.6 Reproduce

The recorder is started in PLAY mode either with the PLAY key on the transport, the PLAY key on a remote control, a fader start device or via software command. The PLAY button turns on.
The PLAY function can be cancelled by pressing the STOP key.
If PLAY is pressed while a recording is in progress, the recorder switches to PLAY mode immediately. If PLAY is pressed during spooling, braking will be initiated, the PLAY functions is preselected, and the PLAY key flashes. As soon as the tape has reached nominal speed, the recorder goes in reproduce mode and the light in the PLAY key is steady.
It is possible to switch from reproduce mode directly to spooling mode or a locator function.
The tape speed (which is proportional to the sampling frequency) can be dictated

- by an external sync source,
- by the reference time track, or
- by any local or remote keyboard (via serial port) in this hierarchical order. Note that playback at the wrong speed is possible if the frequency of the external sync source is not identical to the sampling frequency of the recorded tape. Nominal speed for 48 kHz sampling rate is 15 ips. (0.381m/sec.).

When too much errors are indicated on the quality display (see par. 2.5.27 below), check the red LED's on the Adaptive Run Processor board 1.861.760 located in the box (assembly 4). These LED's should not be flickering in STOP mode. Otherwise, excessive EMI or RFI noise may be picked up by the headblock or associated circuitry from equipment close to the recorder (terminals etc.), causing an increased error rate during playback (see par. 2.2, place of installation).
Another cause for too much errors (especially over splices) may be not correctly adjusted tape tension. Please check with a tentelometer e.g. after RAM failure. Refer to par. 2.5.8, RT SYNC mode, for an other feature to reproduce spliced or track selectively recorded tapes.
The start-up time is elongated for 10.5 and 14" reels when the recorder is loaded with a new tape. Winding the tape will remove this effect. Watch the tape tension guidances for a sudden change in position. The recorder has then adjusted to the new inertia conditions.

2.5.7 Record

RECORD mode is activated by simultaneously pressing REC and PLAY. The lamps in or above these two keys turn on.
If REC and PLAY are pressed during spooling, braking of the tape is initiated. The record function is preselected and the REC and PLAY keys flash. As soon as the tape has reached nominal speed, the D820X enters record mode and the illumination of the two keys is steady.
It is possible to switch from record mode directly to spooling or a locator function.
Recording on the corresponding channel can be disabled by pressing the SAFE key. The yellow SAFE lamp turns on. When REC and PLAY are subsequently pressed, the tape transport starts, however, the audio signals recorded on the track protected with SAFE are retained and can be monitored (reproduce or REHEARSAL mode).
In order to prepare a channel for recording, the corresponding READY key must be pressed. The green pilot lamp turns on. When the recording function is activated with REC and PLAY, the red REC lamp turns on, signalling that recording mode has been activated.
During a recording the channels can be protected directly with SAFE. In order to reenable them for recording, the READY buttons must be pressed first; after the READY

lamps turn on, either the REC and the PLAY keys or only the REC key has to be pressed, depending on the internal programming (RECORD A/B).
The cue track(s) are automatically updated according to the last recording. In single channel record mode and with a single cue channel (aux4mix), only the last recording is written on the cue channel. There is no mix of old recordings with overwritings or punch-in's.

Note: in new record mode, i.e. when a virgin or bulk erased tape is recorded, the keys RECORD and PLAY are to be pressed simultaneously, or better RECORD first and PLAY later. If PLAY is activated first and RECORD later, the recorder stops, because it has not been able to read the content of the reference time (RT) track. The System Controller needs some time to upate its reference time status.

Overwriting of recordings with the tape running upside down (e.g. when a tape which has been stored tail-out is placed on the recorder without rewinding) may cause difficulties when the record current of track 11 (cue right or aux data) has been excessive compared to the normal current used to write reference time (RT). In this case RT can not be overwritten and the recorder stops recording. It may be necessary to bulk-erase the tape or to reverse it. Any attempt to write a tape without valid reference time is prevented, because such a tape would not confirm to the DASH format.
It also may be necessary to check the recording current setting (RECORD CURRENT A/B, in the alignment menu) in order to obtain low error rates (e.g. after using a vastly different tape brand). Par. 1.6, technical specifications, gives information on RECORD CURRENT B settings for certain tapes.
Some function keys are activated only when REC and STORE are pressed together: STOP ADAPTATION, REFERENCE EQ TABLE and when different settings for RECORD CURRENT A or B are entered.

2.5.8 RT Sync Mode

During reproduce, the D820X derives its synchronization signal to read data from tape either from those data themselves or from the reference time (RT) track. Data sync is normally used for stereo operation, i.e. when both channels have been recorded at the same time. It gives superior synchronization performance because 8 tracks contribute to the derivation of a stable sync signal.
RT SYNC mode, however, is recommended for single channel record or playback. Two functions are carried out by this key: a) it protects the reference time track (aux 2) from overwriting (safe function) and b) it selects the synchronizing source for servo control and (to a limited degree) for the time base corrector to be derived from the reference time track and not from an average of the sync patterns of the data tracks. Additionally, splice detection is not carried out by investigating either the occurence of block syncs within a certain time window nor discontinuities of block addresses.
RT SYNC mode is to be used for single channel record mode (sync record) or when a track sequential recording is reproduced and for operation with electronic editors. RT SYNC is automatically selected during single channel record mode and from the electronic editor Studer DE4003. It could also give better performance when spliced tapes are played back, particularly when the splices have poor quality. The synchronization performance may be slightly less reliable when RT SYNC mode is selected, compared to data sync.
In new record mode, i.e. when a blank tape is recorded or when an already recorded tape is completely overwritten, reference time must be recorded, according to the DASH format. The recorder stops if no reference time is recognized in record mode (see par. 2.5.7 above). Therefore the user is advised to record both main (digitalaudio) channels even if only one contains valid information (RT SYNC off). Then reference time (and cue) will be written and the synchronization signal to read data is derived from data for more reliability. Servo control is always derived from the crystals in RECORD mode.

Described below are some more detailed considerations concerning single channel recording: the time base corrector is controlled by reference time and the already written reference time is preserved. The new track is aligned to reference time according to the DASH format, provided that the head distance is correctly adjusted. The sync words from both channels may be displaced by up to 1 block (each track ± 1 block) referenced to reference time due to tape transport instabilities (wow & flutter), when one track is read and the other is written. This large displacement is the reason why RT SYNC gives a better performance for track sequential recordings, because otherwise (when written at once), the spread of the sync patterns is largely determined by the head geometry. In case of a non-continous reference time (e.g. after a splice) a reaction time of 157 blocks has to be taken into account, before the block numbers again correspond to the sectors (152 blocks head distance plus 4 blocks delay in the data synchronizer plus 1 block formatter delay).

PLAY (KEY "RT SYNC" ENABLED)		RECORD (KEY "RT SYNC" DISABLED)		
X	SERVO CONTROLLED BY DATA	Y		SERVO CONTROLLED BY RT ! (*)
X	RT MODE: READ RT	Y		RT MODE: READ ONLY ! (*)
X	LED "RT SYNC": OFF	Y		LED "RT SYNC": FLASHING (*)
Z	SERVO CONTROLLED BY RT	T	U	SERVO CONTROLLED BY CRYSTAL
		T	U	RT MODE: WRITE RT
		T	U	LED "RT SYNC": OFF
Z	RT MODE: READ RT			
		T	V	SERVO CONTROLLED BY RT (**)
		T	V	RT MODE: READ ONLY
Z	LED "RT SYNC": ON	T	V	LED "RT SYNC": FLASHING

X = KEY "RT SYNC" OFF
Z = KEY "RT SYNC" ON
Y = CH 1 OR CH 2 SAFE
T = CH 1 AND CH 2 READY
U = KEY "RT SYNC" OFF
V = KEY "RT SYNC" ON
(*) = independent of key "RT SYNC"
(**) = it the tape contains no RT, the tape deck establishes "STOP" mode and the message "no reference track" is displayed.

2.5.9 Spooling, Shuttle

Fast forward or rewind is activated by pressing ► and ◄. The recorder spools with the programmed speed (max. 15m/sec.). The default value for normal wind speed is 10 m/sec. in normal WIND mode and 2.5 m/sec. in LIBRARY WIND mode. Precision reels are recommended for good spooling behavior. With other reels the spooling behavior may be improved by reducing the wind speed. Shuttle: the wind speed is proportional to the inclination of the shuttle wheel (no wind speed in idle position). The wind speed is stored by pressing the shuttle bar. The tape is in contact with the heads, permitting a fast search of tape positions by additionally monitoring the cue or time code track(s).

The spooling functions are canceled by STOP, PLAY, REC+PLAY, SHUTTLE, LOC functions, CUE, and by spooling in the opposite direction.

Direct change-over from rewind to fast forward and vice versa or from playback or recording to spooling is possible.

It is also possible to switch from spooling mode directly to record and play. The pilot lamp of the preselected function flashes, the tape is braked, and the new function is activated as soon as the tape travels at the nominal speed.

Tape lifter off: during spooling the tape is automatically lifted off the heads in order to reduce wear.

The tape transport assembly can be engaged by pressing the LIFTER button (if assigned to a key).

The parameter (value) displayed in the alignment deck menu shows maximum possible wind speed for all wind modes except LIBRARY WIND mode. The recorder therefore

ensures secure tape handling. A higher speed value (requested by i.e. remote controllers) than that locally defined is limited. The maximum speed value can only be changed locally, from the menu of the recorder or by activating LIBRARY WIND.
When LIBRARY WIND with a lower speed value than in normal WIND mode is selected the preset LIBRARY WIND speed is immediately active. The same action takes place when changing from LIBRARY WIND to normal WIND mode. The only exception is activating normal WIND or LIBRARY WIND after a WNF or WNR command from the serial port. Execution of the slower wind speed takes place only in succession of another WNF or WNR command.
When LIBRARY WIND is selected with a higher speed value than in normal WIND, spooling speed is increased and vice versa.

Caution! During fast wind operations the console tilting mechanism must not be actuated - tape, reels, reel adaptors, and tape transport cover may be seriously damaged as a result of the high gyro forces!

2.5.10 Library Wind (Reduced Spooling Speed)

The reduced spooling speed available with the LIBRARY WIND function is intended for tapes that are to be stored in a library. The speed ranges between 0.1 and 15 m/sec. and can be programmed in increments of 0.1 m/sec., (default: 2.5 m/sec.). The parameter (value) displayed in the alignment deck menu shows maximum possible wind speed. Spooling with reduced speed is initiated by pressing the LIBRARY WIND key and one of the spooling keys ◄ or ►. The function is stopped by pressing LIBRARY WIND a second time.
The recorder therefore ensures secure tape handling. A higher speed value (requested by i.e. remote controllers) than the one locally defined is limited. The maximum speed value can only be changed locally, from the menu of the recorder (alignment deck menu).
When LIBRARY WIND with a lower speed value than in normal WIND mode is selected the preset LIBRARY WIND speed is immediately active. The same action takes place when changing from LIBRARY WIND to normal WIND mode. The only exception is activating LIBRARY WIND after a WNF or WNR command from the serial port. The executing of the slower wind speed takes place only in succession of another WNF or WNR command.
When LIBRARY WIND is selected with a higher speed value than in normal WIND, spooling speed is increased and vice versa.

2.5.11 Stop

The STOP key has top priority and cancels all other operating modes such as reproduction, recording, spooling, and autolocator. After this key has been pressed, the STOP pilot lamp turns on and tape braking is initiated; the STOP key flashes until the tape stands still after which the illumination of the STOP key becomes steady.
When the tape stands still the tape tension control loop, however, is active (exception: tape torn or unthreaded). This makes it easier to shuttle the tape by hand for editing purposes. Any new operating mode entered while the tape is being decelerated will be stored and activated as soon as the tape reaches nominal speed.
If STOP is pressed and (while STOP is held) also one of the keys LOC1...LOC5, the corresponding locator addresses are displayed on the tape counter.

2.5.12 Locators

The following modes are complemented by functions available exclusively with the autolocator:

- ZERO LOC: zerolocator. This key initiates a rewind (or fast forward) to the tape address that corresponds to the counter reading 0.00.00.0, as well as for the main as for the second counter display (absolute and relative time).
- LOC START (programmable): this key initiates a rewind (or fast forward) to the tape address at which the last play command was entered during standstill of the tape. Depending on the programming either STOP (function LOC START STOP), reproduce (function LOC START PLAY) or recording (function LOC START REC) is activated. Default programming: LOC START PLAY.
- LOC1...LOC5 (programmable): transfer locator. Up to five tape positions can be stored and automatically searched in spooling mode by pressing one of these keys.

The locate procedure can be interrupted with: ◄, ►, STOP, EDIT, or 2 x PLAY.

Programming: Search the desired tape address and press the TRANS key when the approximate position has been reached. The address can be stored as long as the TRANS pilot lamp is on. As soon as the exact position has been found, press one of the corresponding LOC keys. The TRANS pilot lamp turns off to acknowledge that the address has been transferred into memory. The TRANS key must be pressed again before a new address can be stored.

Reading out an address: during a LOC operation: by pressing the corresponding LOC button again. In STOP mode: press STOP and corresponding LOC button. PLAY or REC preselection: if the PLAY key is pressed (or PLAY + REC) while a locate function is in progress (ZERO LOC, LOC START, LOC1...5), the recorder switches automatically to reproduction or to recording after the corresponding tape address has been found.

All locate addresses are retained in memory even after the recorder has been switched off.

A special condition exists when a locate command is executed to an address beyond or below the capabilities of the tape. The recorder behaves according to the parameter stored in the TAPE GUARD function (KEY/MODE SETTINGS TAPE DECK):

- when no guard is selected, the tape will thread out; tape deck status is tape-out. The function is cancelled.
- with tape guard set to reduced, the functional behavior is identical, but slower.
- with tape guard set to stop, the recorder enters STOP mode. Tape deck status is stop. For an external controller (e.g. a synchronizer) there will be no difference between stop status forced by the tape guard function and stop status entered after successful execution of a LOCATE function.

Caution! Since the stored tape addresses relate to the actual tape positions, any undesirable offsets can occur if the RESET TIMER button is pressed inadvertently!

2.5.13
Time, Reset Timer

2.5.13.A

Tape Counter

The electronic tape counter always displays the real (absolute) time in hours, minutes, seconds, and tenths of seconds, regardless of the selected nominal speed.
The display capacity is -9 h 59 min 59.9 s to 23 h 59 min 59.9 s. Values outside the display capacity are indicated with "u" (underflow) and "o" (overflow) in the tens-of-hours position; e.g. o4.00.00.0 or u9.59.58.0. Fractional tenths of seconds are rounded to the nearest second when the appropriate display format is used (see functions "set LED stop format", "set LED move format" and "set leading zeroes" in the alignment deck menu). The timer can be reset to 0.00.00.0 by pressing the RESET TIMER key.
When the end of the tape is reached or if a tape tears, the tape counter is automatically stopped. In dump edit mode (TAPE DUMP) the tape counter is either stopped automatically or it continues to count, depending on which of the four TAPE DUMP modes has been programmed (standard programming: TAPE DUMP A, the counter continues to count with the information obtained from the capstan motor tacho).
The display format for all TIME displays can be altered in the alignment deck meny with functions "set LED stop format" (suppresses right justified numbers in STOP mode), "set LED move format" (suppresses right justified numbers in PLAY, RECORD, EDIT, CUE, SHUTTLE, LOC and WIND modes) and "set leading zeroes" (valid for all tape deck modes).

2.5.13.B

Watch

By pressing the WATCH key (standard programming on the display panel) the tape counter display can be switched over from the main counter to indication of a second tape counter with arbitrarily selectable reference (relative time). An "I" appears in the first position of the display.
The second counter can be set to zero at any tape address (with RESET TIMER button) and can, for example, be used for measuring the exact playing time of a selection without having to compute the difference between the starting and the ending time.
The display is switched back to normal mode by pressing the WATCH key a second time. The "I" in the first position disappears.
Locator addresses are referred to the tape positions and are preserved when switching to WATCH mode (and back to normal tape counter mode).
WATCH mode is automatically selected in "show quality" mode from an externally connected terminal or computer. Do not leave WATCH mode as long as tape errors are accumulated.
The display format for all TIME displays can be altered in the alignment deck meny with functions "set LED stop format" (suppresses right justified numbers in STOP mode), "set LED move format" (suppresses right justified numbers in PLAY, RECORD, EDIT, CUE, SHUTTLE, LOC and WIND modes) and "set leading zeroes" (valid for all tape deck modes).

2.5.13.C

Reference Time

It is a dedicated track for an internal time which is synchronous with digitalaudio. Display: press TIME three times (when programmed as ring key); reference time (RT) is marked with a leading "r". The track basically needs no operational control. Its built-in generator runs continously and can be reset with the RESET TIME key.
See chapter 2.5.19 for more specific information on RT.
The display format for all TIME displays can be altered in the alignment deck meny with functions "set LED stop format" (suppresses right justified numbers in STOP mode), "set LED move format" (suppresses right justified numbers in PLAY, RECORD, EDIT, CUE, SHUTTLE, LOC and WIND modes) and "set leading zeroes" (valid for all tape deck modes).

2.5.13.D

Time Code

There is a dedicated time code track, AUX 1, the lowest track of the head stack. Time code according to the SMPTE standard is recorded from an external generator. The time code output is aligned (but not time base corrected) with digital- or analogaudio, provided that the frame rate has been properly selected (according to generator or tape) and that the delay is activated (see functions 401...406 and 425, 426 in the TC menu). Not only time but USER or UNASSIGNED BITS can be displayed with the TIME key as selected in the above mentioned menu.
Time code input can be monitored by pressing INPUT on the TC column of the Channel Control panel. Audible off-tape monitoring is provided with the TC key on the Monitor panel.
Refer to par. 2.5.18 or key 401 ff. for more information.
The display format for all TIME displays can be altered in the alignment deck meny with functions "set LED stop format" (suppresses right justified numbers in STOP mode), "set LED move format" (suppresses right justified numbers in PLAY, RECORD, EDIT, CUE, SHUTTLE, LOC and WIND modes) and "set leading zeroes" (valid for all tape deck modes).

2.5.14 Remote Controls

The following functions can be activated from the parallel remote control: reproduction, recording, spooling, stop, RESET TIMER, ZERO LOC, LOC START, RECAP (rewind for as long as this key is pressed, followed by PLAY) or LIFTER (canceling of the tape lift during spooling), and FADER (FADER START ready).
It is possible to assign all the functions to the keys of the serial remote control that can be programmed for the local keyboard, but independent of the programming of the local keyboard. I.e. different key functions as on the local keyboard may be programmed on the serial remote control. In addition the serial remote control features a tape counter and a SHUTTLE wheel. The programming of the key functions is executed in the same way as for the local keyboard.

- Operation with programmable function REMOTE A: when the REMOTE key is pressed, the corresponding pilot lamp turns on and the local keyboard is disabled. When the REMOTE key is pressed a second time, the local keyboard is reenabled and the pilot lamp turns off. In the latter condition the keys on the remote control have no effect.
- Operation with programmable function REMOTE B: when the REMOTE key is pressed, the corresponding pilot lamp turns on; the remote control buttons and the local keys have equal priority. When the REMOTE key is pressed a second time, only the local keys are active and the pilot lamp turns off. In the latter condition the keys on the remote control have no effect.
- Operation without the functions REMOTE A and REMOTE B: the REMOTE LED is always turned on, the keys on the local and on the remote keyboards are always active.

2.5.15 Fader

Four programming modes:

Fader A: without preparation key (FADER START READY)

Fader B: FADER START with enable key (FADER START READY), local keyboard also active when FADER START enabled. The local keyboard will be disabled after FADER START; default programming.

Fader C: Same as FADER START B, except local keyboard disabled when FADER START enabled.

Fader D: FADER START with enable key (FADER START READY), local keyboard also active when FADER START enabled. After the FADER START, the built-in monitor speaker (not the headphones, however) is muted. If one of the local keys is operated in PLAY mode after the FADER START operation has been performed, muting of the monitor speaker is canceled. If FADER START is not enabled, actuation of the FADER switch does not change the operating mode of the recorder.

With the fader start circuit, the recorder can be started in PLAY mode from the remote control device. FADER START can be prepared (FADER START READY) by a switch that interconnects contact 6 (signal SR-FADRY) and contact 1 (ground). Applying an AC or DC voltage from 5 V to 24V to contacts 11 and 12 switches the tape recorder to reproduce mode. This preparation can also be made with the programmable FADER key on the local keyboard or the serial remote control, or with the FADER key on the parallel remote control.

General note:

In the description below the local and remote keyboards are mentioned. This concerns all keys on the tape deck and on remotes. All these keys may be disabled with the exceptions mentioned below.

When fader start is activated, all transport error modes, unload, power-down and tape-out commands remain active, ensuring smooth tape handling in every case.
Only one fader type (A...D) is enabled. If the programming is changed from the keyboard or from one of the remotes, the new setting and function is active and the old setting and function is released.
The fader functions (FADER A...D) are independent on the remote settings NO REMOTE, REMOTE A or REMOTE B.

1. FADER START A

In this version, the recorder has no "fader start ready" key.
As soon as the fader connectors FAD1/FAD2 are activated, the recorder is in PLAY mode and the local and remote keyboards are disabled with the exception of key EMPHASIS and the CURSOR keys. The tape deck monitor and the monitor panel are muted. The phone connector is still active.
When the fader connectors FAD1/FAD2 are desactivated, STOP mode is initialized and the tape deck monitor and the monitor panel are demuted as soon as STOP is achieved. Otherwise normal operation is established.
Tape-out/unload/TD-error/power-down: FAD1/2 desactivated. When after tape-out/unload/TD-error/power-down the key PLAY is pressed and the fader connectors FAD1/2 are activated, the recorder establishes normal play mode (monitor panel demuted). When now the fader connectors FAD1/2 are desactivated, normal play mode continues. Only after the fader connectors FAD1/2 are activated again, normal fader operation is established as described in this paragraph.

RECORD mode: FAD1/2 connector is ignored.
TAPE DUMP A...D: FAD1/2 connector ignored.

2. FADER START B

In this version an internal and/or external "fader start ready" key is present.
When key "fader start ready" is not closed (signal SR-FADRY not present), any activation of the fader connectors FAD1/FAD2 is ignored. The local and remote keyboards remain activated, independent on the state of the fader connectors FAD1/FAD2. Normal operation.
When key "fader start ready" is closed (signal SR-FADRY present) and the fader connectors FAD1/FAD2 are activated, the recorder is in PLAY mode and the local and remote keyboards are disabled with the exception of key EMPHASIS and the CURSOR keys. The tape deck monitor and the monitor panel are muted. The phone connector is still active.
When the fader connectors FAD1/FAD2 are desactivated, STOP mode is initialized and the tape deck monitor and the monitor panel are demuted as soon as STOP is achieved. Otherwise normal operation is established. The fader functions are enabled dependent on the state of the "fader start ready" key.
Tape-out/unload/TD-error/power-down: FAD1/2 desactivated. The "fader start ready" key is still active. When after tape-out/unload/TD-error/power-down the key PLAY is pressed and the fader connectors FAD1/2 are activated, the recorder establishes normal play mode (monitor panel demuted). When now the fader connectors FAD1/2 are desactivated, normal play mode continues. Only after the fader connectors FAD1/2 are activated again, normal fader operation is established as described in this paragraph.

RECORD mode: FAD1/2 connector is ignored.

TAPE DUMP A...D: FAD1/2 connector ignored.

3. FADER START C

In this version an internal and/or external "fader start ready" key is present.
When key "fader start ready" is not closed (signal SR-FADRY not present), any activation of the fader connectors FAD1/FAD2 is ignored. The local and remote keyboards remain activated, independent on the state of the fader connectors FAD1/FAD2. Normal operation.
When key ""fader start ready" is closed (signal SR-FADRY present), the local and remote keyboards are disabled, with the exception of key EMPHASIS, the CURSOR keys and the "fader start ready" key.
When key "fader start ready" is closed (signal SR-FADRY present) and the fader connectors FAD1/FAD2 are activated, the recorder is in PLAY mode and the local and remote keyboards remain disabled with the exception of key EMPHASIS and the CURSOR keys. The tape deck monitor and the monitor panel are muted. The phone connector is still active.
When the fader connectors FAD1/FAD2 are desactivated, STOP mode is initialized and the tape deck monitor and the monitor panel are demuted as soon as STOP is achieved. The fader functions are enabled dependent on the state of the "fader start ready" key. Local and remote keyboards remain desactivated (except key EMPHASIS and the CURSOR keys) until key "fader start ready" is released.
Not bevore key "fader start ready" is disabled will the recorder establish normal operation again.
Tape-out/unload/TD-error/power-down: FAD1/2 desactivated. The "fader start ready" key is inactive. When after tape-out/unload/TD-error/power-down the key PLAY is pressed and the fader connectors FAD1/2 are activated, the recorder establishes normal play mode (monitor panel demuted). When now the fader connectors FAD1/2 are desactivated, normal play mode continues. Only after the fader connectors FAD1/2 are activated again, normal fader operation is established as described in this paragraph.

RECORD mode: FAD1/2 connector is ignored.

TAPE DUMP A...D: impossible, when key "fader start ready" is active. The key "fader start ready" is ignored, when the recorder is in mode TAPE DUMP A...D.

4. FADER START D (Finnland)

In this version an internal and/or external "fader start ready" key is present.
When key "fader start ready" is not closed (signal SR-FADRY not present), any activation of the fader connectors FAD1/FAD2 is ignored. The local and remote keyboards remain activated, independent on the state of the fader connectors FAD1/FAD2. Normal operation.
When key ""fader start ready" is closed (signal SR-FADRY present), the local and remote keyboards remain enabled. All transport functions remain enabled (error modes!).
When key "fader start ready" is closed (signal SR-FADRY present) and the fader connectors FAD1/FAD2 are activated, the recorder is in PLAY mode and the local and remote keyboards remain enabled. The tape deck monitor and the monitor panel are muted. The phone connector is still active.
To exit from this mode: press any transport key. All commands from the tape deck (tape out, errors, etc.) are enabled. Then the tape deck monitor and the monitor panel are demuted. When the fader connectors FAD1/FAD2 are desactivated, STOP mode is initialized and the tape deck monitor and the monitor panel are demuted as soon as STOP is achieved, unless any transport key or tape deck command has been activated before. The condition for demuting therefore is: any transport key pressed or STOP achieved. If any transport key or tape deck command has been activated before the FAD1/FAD2 signal is removed, the FAD1/FAD2 command is ignored. Normal operation is established.
Tape-out/unload/TD-error/power-down: FAD1/2 desactivated. The "fader start ready" key is still active. When after tape-out/unload/TD-error/power-down the key PLAY is pressed and the fader connectors FAD1/2 are activated, the recorder establishes normal play mode (monitor panel demuted). When now the fader connectors FAD1/2 are desactivated, normal play mode continues. Only after the fader connectors FAD1/2 are activated again, normal fader operation is established as described in this paragraph.

RECORD mode: FAD1/2 connector is ignored.

TAPE DUMP A...D: FAD1/2 connector ignored.

2.5.16 Cue Track(s)

The tracks AUX 3 and AUX 4 (if assigned to cue) carry the same information as the main tracks. Not in digital form, however, but recorded with (analog) PDM modulation. Due to this, monitoring of the same information as recorded on the main tracks is possible over a wide speed range. The modulation index and the carrier frequency have been chosen to show close resemblance with HDM-1 modulation regarding power spectral density. This ensures that heads and tape are operated in regions of highest efficiency. Full compatibility exists with conventional bias or direct recording methods.
A flag in the reference time control word indicates whether the cue tracks have been recorded originally in modulated or unmodulated form. Playback of recordings with a deliberate mismatch between the indication on the reference time track and the desired playback method, are made possible with keys 046 and 047 (see keys CUE: UNMODULATED/AUTO and CUE: MODULATED/AUTO). The assignment of auxiliary track 3 to data or cue is performed with keys 044 and 045.
For audio routing of cue signals see 2.5.13, Monitor panel.
There is no external input for the cue tracks except for auxiliary track 3, when assigned to a data track with key ASSIGN AUX3: DATA/CUE.
The cue track(s) are automatically updated according to the last recording. In single channel record mode and with a single cue channel (aux4mix), only the last recording is written on the cue channel. There is no mix of old recordings with overwritings or punch-in's.

2.5.17 AUX3 Track

The auxiliary 3 track may carry external data when key 044 is in position "data". The pilot LED "aux4mix" is illuminated and the column of keys labeled "AUX" on the Channel Control panel is activated. With the keys of this column the usual SAFE/READY and INPUT/REPRO functions are possible (see description of corresponding keys). When function 044 is not in position "data" the track carries cue information (right channel).
The setting of key 044 is written on the reference time track and the recorder configures itself according to this flag. The automatism can be suppressed with key 045: AUX3+4: MANUAL/AUTO (see description of this key).
External data written on this track is not protected by the recorder itself. A conventional direct recording method with pulsed write current is used. The adjustment of the write current is adjusted for best performance with (modulated) cue signals.
The main purpose of this track with its fairly large bandwidth (see par. 1.6 and 1.7) is to store subcode data for CD tape and disk mastering.

2.5.18 Time Code Track

The D820X accepts external time code (TC) from a remote generator connected to the time code input connector (XLR type). No internal link exists between this input and the videoclock input. When synchronism to video or digitalaudio is required, the external generator must be gen-locked to an appropriate sync signal (simple multiple ratio to word or frame clock, etc.) and a simple integer ratio must exist between the sampling frequency and/or the time code frame rate according to the table below.

Video-/Film-Clocks VS. Sampling Frequencies

ORIGIN	LINES	FRAMES	RELATIONSHIP TO SAMPL. FREQUENCIES			
		sec.	32	44.1/1.001	44.1	48
NTSC monochrome	525	30	(15/16)	---	1470	1600
NTSC color	525	30/1.001	---	1470	---	(8008/5)
PAL monochr./col.	625	25	1280	---	1764	1920
FILM	---	24	---	---	---	2000

Time code recording:

Press the READY button on the time code column of the Channel Control panel; the READY lamp and the pilot lamp TC READY turn on. Start the D820X in record mode with REC and PLAY; the REC lamp turns on. Or, while a recording is in progress, press READY and, depending on the programming, press REC + PLAY or just REC.
Local TC display and the corresponding information available via serial port is interpolated in wind mode and during dropouts with pulses from the move roller. A point to the right of prefix "t" appears when this takes place. Select the appropriate delay to align TC frames with digitalaudio data and to obtain an accurately interpolated display by means of functions 401...406 in the menu, according to the incoming frame rate or/and to the frame rate on tape. The choosen frame rate is displayed in the standard LCD menu picture for convenience.

Time code reproduction:

Start the D820X in playback mode by pressing PLAY. The recorder will output non-interpolated serial TC data at the TC output (XLR connector) and it displays interpolated TC on the LED display(s). Selection of CODE, USER BITS or UNASSIGNED BITS is dependent on the programming of functions 407...411 (see table below).

TC Display Format

POSITION	0	9	8	7	6	5	4	3	2	1	
MODE 1:	A	H2	H1	M2	M1	S2	S1	F3	F2	F1	CODE
MODE 2:	A	U8	U7	U6	U5	U4	U3	U2	U1	U	USER BITS (HEX CHARACTERS)
MODE 3:	A	–	–	0	9	8	7	6	5	F	UNASSIGNED BITS (BIN. DIGITS)
ADDRESSES:	49	47	45	43	41	39	37	35	33	31	

F = FRAMES
A = (t) TC

U = USER BITS
F = FLAGS

U8 = BINARY GROUP 8
U7 = BINARY GROUP 7
U6 = BINARY GROUP 6
U5 = BINARY GROUP 5
U4 = BINARY GROUP 4
U3 = BINARY GROUP 3
U2 = BINARY GROUP 2
U1 = BINARY GROUP 1

0 = BIT 59
9 = BIT 58
8 = BIT 43
7 = BIT 27
6 = BIT 11 (COLOR FRAME FLAG)
5 = BIT 10 (DROP FRAME FLAG)

Note: ASCII-Characters are not displayed.

Time code readout is set automatically according to a flag on the reference time track. Studer recorders always record TC in PDM modulated form and set the playback circuit to reproduction of modulated data. For playback of tapes containing analog modulated time code, but with a flag set to modulated time code (i.e. when an originally modulated TC has been restriped with unmodulated TC from a recorder of different origin), the TC flag can be overwritten by selecting TC UNMODULATED (functions 415 and 416). Conflicting situa- tions may arise because reference time is updated together with digitalaudio data only.
The output delay may be bypassed (no delay) when function 425 is set to off. In auto mode the delay is active in PLAY or REC mode and bypassed in EDIT, CUE, SHUTTLE, LOCATE and wind modes, because monitoring of cue tracks only is possible in these modes and since there is no delay when cue tracks are reproduced, the TC display is coincident when no delay is inserted.
When TC display is delayed, the indication is aligned with digital- or analogaudio, except for 44.1 kHz sampling rate, where an offset of 11 milliseconds exists with RT/TC Codec 1.861.761.21. The table below gives ideal delay values which are obtained with boards of index -22 and up and indicates differences to the -21 version.

Time Code Delays VS. Digitalaudio Delays

CELLS | BLOCKS / DELAY [msec.]	REPRO DELAY OFF		25 FR.		29, 30 Fr.	
48 kHz	---	166.5	477	238.5	572	238.5
	83		120		120	
44.1 kHz 44.056 kHz	---	166.5	521 (1)	238.5	624 (2)	238.5
	91		131 (3)		131 (3)	
	←INPUT DELAY→		←REPRO DELAY→			

The numbers above are exact values.

Errors with board RT/TC CODEC 1.861.761.21:
(1) ERROR = 44 CELLS = 1/4 FRAME
(2) ERROR = 52 CELLS = 1/3 FRAME
(3) ERROR = 11 msec. (120 msec. IMPLEMENTED).

2.5.19 Reference Time Track

The reference time (RT) track carries time information which is strictly synchronous with digital data. The "frames" of the RT track are called sectors and each sector has a unique (time) address, provided that no multiple addresses exist. The duration of a sector corresponds to four blocks, and the start of each sector is aligned with the beginning of block with number 00. The sector rate therefore is 2000 Hz for 48 kHz sampling rate. RT is mandatory when single channels are to be written and the D820X requires RT only in this application, together with key RT SYNC active. Other recorder designs use RT also for servo control and to detect splices.

RT permits the identification of each block, even of single words, due to its synchronism with digitalaudio. Such an accuracy with respect to resolution is made possible through the alignment of RT with digitalaudio on tape as well as at the outputs of the recorder. The RT output (XLR type) of the D820X is time base corrected and accurately aligned with digitalaudio to support exacting synchronization and editing operations. RT is written with biphase modulation and the output is formatted identically as the signal on tape (see DASH format and 1.7, interfacing specifications).

All DASH tapes require reference time. The D820X has been designed to inhibit recording without a reference track (see also par. 2.5.8: RT SYNC mode).

RT is generated internally and can be reset with the RESET TIME key when the display shows reference time, marked with prefix "r". It is recorded only once: during initial or "new" record (see key RT SYNC). In append record mode, RT is jam synced, when the recorder has been given some time to read previously written RT. No discontinuity in time addresses will then occur.

RT not only carries time information but also control words which are used for automatic set-up and are necessary for tape interchangeability purposes (see table below): a flag indicating twin format, three bits for sampling frequency, three bits for the format version (i.e. 001 indicates DASH M, normal density), three bits indicating the use of the auxiliary tracks and six reserved bits.

The bits indicating the use of the auxiliary tracks are especially important. One bit indicates conventional or modulated recorded cue tracks, another specifies whether track aux3 contains data or cue information and the last bit separates between conventional or modulated recorded time code (aux1). Studer recorders always record modulated cue tracks and time code.

From this control word information on the reference time track (which is not updated during overdubs) some difficulties may arise when the overdub has been made with a recorder using a different recording method for cue and/or time code then the initial recorder. Consider the case when conventional direct or bias recording method was utilized originally and when the data tracks of such a tape are overwritten with a D820X recorder. The reference track will still contain the old (invalid) data although the cue and time code track(s) could have been overwritten with PDM modulation. In order to reproduce this tape, the functions 047 "CUE: MODULATED/AUTO" and 416 "TC: MODULATED/AUTO" are provided in the menu and should be set to modulated in this example.

Reference Time

BYTE NO	SIG NAME	DESCRIPTION BITS	7	6	5	4	3	2	1	0
1 (91H)	FLAG	SET TO 1 FOR TWIN FORMAT	1							
	SAMPFREQ	SAMPLING FREQUENCY TO RT/TC CODEC		M	B	L				
		000 UNSPECIFIED								
		001 48kHz NOMINAL								
		010 44.1kHz NOMINAL								
		011 32kHz NOMINAL								
		100 44.056kHz								
		101...111 RESERVED								
1 (91H)	FORMAT	DASH FORMAT VERSION					0	0	1	
		001 INDICATES DASH M, NORMAL DENSITY								
1 (91H)	AUXTRKFO	AUX TRACK FORMAT								0
2 (93H)	AUXTRKFO	AUX TRACK FORMAT	0	1						
		XX0 INDICATES ANALOG CUE TRACKS								
		XX1 INDICATES PDM CUE TRACKS								
		X0X INDICATES AUX3 NO AUX DATA								
		X1X INDICATES AUX3 AUX DATA								
		0XX INDICATES TC UNMODULATED								
		1XX INDICATES TC MODULATED								
		(ALL UNLESS OTHERWISE SPECIFIED)								
2 (93H)	RESERVED	RESERVED BITS			0	0	0	0	0	0
		NOT YET SPECIFIED, SET TO 000000								
3 (95H)	RTATOC01	RT ADDR 1 WITH OFFSET FROM SYSCON	M	6	5	4	3	2	1	0
4 (97H)	RTATOC02	RT ADDR 2 WITH OFFSET FROM SYSCON	7	6	5	4	3	2	1	0
5 (99H)	RTATOC03	RT ADDR 3 WITH OFFSET FROM SYSCON	7	6	5	4	3	2	1	0
6 (9BH)	RTATOC04	RT ADDR 4 WITH OFFSET FROM SYSCON	3	2	1	L	X	X	X	X

When the tape suddenly stops in RECORD mode, check the RT TIME display. If it reads "no rt track", then the HDM/RUN jumper connector on the Write Amplifier may be in the wrong position (RUN) or the write head is not connected at all. Otherwise check the individual write current settings of the Write Amplifier and the offset settings in the alignment audio menu ("record current A/B"). If all fails the fault must be located on the Write Amplifier (located in the cage behind the headblock), the RT/TC Codec board (located in the box, assembly 4), or in the first playback amplifier stages.
RT readout and update of RT Control Word in "synchronizer on" mode: due to possible instabilities there is no Reference Time readout as long as SYNC IN SYNCHRONIZER is selected. The last valid RT Control Word is frozen, meaning that sampling frequency, format version and auxiliary track format information is not updated during the chase phase.

2.5.20 Tape Deck Monitor (Version -2)

The internal monitor which comes with a built-in mono speaker located in the tape transport is equipped with controls as shown below:

Keyboard Tape Deck Monitor:

	INPUT		DIGITAL		
*	*	*	*	*	*
VOLUME	TAPE	TC	CUE	1/MIX	2/AUX

After the volume potentiometer there is an INPUT/TAPE key, similar in performance to the INPUT/REPRO key on the Channel Control panel or functions 010 and 011 in the menu. The TC key is a non- locking type which allows audible monitoring of the time code track when the button is pressed. The next key, DIGITAL/CUE allows listening to the main (digitalaudio) channels in position DIGITAL. In position CUE either the left cue track (1) or a mix of both cue channels (menu function 044 set to "data") is selected. This key is not interlocked with the next, 2/AUX, both can be pressed together for monitoring of both cue chanels (1 and 2), when function 044 is in position "cue". Otherwise the key 2/AUX allows listening to the auxiliary data track in position AUX.
The internal Tape Deck Monitor is fitted in recorders without panel (version D820X-2).

2.5.21
Channel Control Panel (Version -2PPM)

Functions:
- SAFE and READY keys
- RECORD indicator
- INPUT and REPRO keys
- RT SYNC key.

SAFE, READY

Each channel or track (CH 1, CH 2, AUX, TC) can be enabled (READY) or disabled (SAFE) for record mode. The selected mode is indicated by an LED in the keys (yellow for SAFE, green for READY). The auxiliary track is enabled in aux4mix mode (see description of function 044, ASSIGN AUX3: DATA/CUE, chapter 2.6).
Record preparation condition: press key READY. The LED will turn on. When key RECORD on the tape deck is additionally pressed: the RECORD lamp turns on and key READY is not illuminated anymore. Note: if the recorder is already in record mode, pressing READY alone is not sufficient for entering recording mode, key RECORD must be pressed again.
Both SAFE and READY keys are accessible in reproduce mode and the appropriate status is displayed.
The functions SAFE and READY are duplicated in the menu (functions 030, 033, 036 and 042) and are functionally treated as described above.

RECORD

The key RECORD on the tape deck and the red LED on the Channel Control panel are illuminated in RECORD mode for all those channels which are not in SAFE mode. Quit record mode with SAFE key. If there is no channel in RECORD anymore, the key RECORD on the tape deck is disabled. The SAFE keys are illuminated when activated and the READY keys disabled. Two different RECORD modes are supported (see functions 307 and 308).

INPUT, REPRO

Each channel or track can individually be set to reproduce or indicate (TC) the INPUT signal or the off-tape signal (REPRO).
When INPUT is selected, the digital output gains are bypassed. They become effective in REPRO mode or with some of the EE-loops (EE1, 2, 3). Refer to function 070: TEST.

RT SYNC

Two functions are carried out by this key:
a) it protects the reference time track auxiliary 2 from overwriting (SAFE function) and
b) it selects the synchronizing source for the time base corrector and for the servo control to be derived from the reference time track and not from an average of all the sync patterns from the 8 data tracks (at least five tracks must contain valid data). The function RT SYNC is provided for recording and playback of channel sequential tapes (single channel record/playback) and - in rare occasions - for playback of mechanically poorly edited tapes.
See par. 2.5.8 for a detailed description of this key.

2.5.22
Display Panel (Version -2PPM)

The structure of the Display panel: it is subdivided into the keyboard at the bottom and four display sectors

- the level display section (bargraphs)
- the signal quality display (16 colored LED's)
- a status display section (below signal quality), and
- the seven-segment LED display for time information, etc.

The Display panel has its own power supply, operating from + 20 VDC generated in the power supply box (assembly 4).
It is interconnected through a 25-way ribbon cable with a Dsub25 connector. The internal control bus which is fed to the panels is terminated at the Display panel. The bus is buffered on the PCB Display IF 1.861.817, located in the right hand side of the rack (assembly 11).

- The level display section on the left hand side (bargraphs) show signal level. One column is provided for each main (digitalaudio) channel. The response is true peak (every sample displayed), with a decay time of 1.5 seconds per 20 dB. Only digitally derived "levels" are displayed: information originating after the analog-to-digital converter and after the digital input gain adjustment in the record path, and after the digital output gain adjustment and before the digital-to-analog converter in the reproduce path.

  The display range is 50 dB in 1 dB increments. The lowest segments are always active to indicate normal behavior.
  Both uppermost LED's show clipping of the analog-to-digital converter and/or digital clipping in the data processor. Digital clipping from the in- and output path is indicated independent on the state of INPUT/REPRO keys.

- 16 horizontally positioned LED show signal quality according to the table below.

Composition of signal quality data

ORIGIN	ADDR	NAME	ABBREV	DESCRIPTION
SYSCON	01	LOW ERROR RATE	OK	NORMAL BEHAVIOR
CODEC	02	QP2 CORRECTION	QP2	SECOND PASS QP-PARITY CORRECTION
CODEC	04	FINGERPRINT	FP	FINGERPRINT >=4 TRKS, T<<
CODEC	08	TRACKLOSS	TL	>=1 TRK, T>=512 BLOCKS (1/4 SEC.)
DAPRO	10	INTERPOLATION 2	INT 2	INTERPOLAT. 2ND GRADE (QUADRATIC)
DAPRO	20	INTERPOLATION 1	INT 1	INTERPOLAT. 1ST GRADE (LINEAR)
DAPRO	40	MUTE	M)	MUTE WITH TIMEOUT 0.5 SEC.
SYSCON	80	NO DATA	ND)	AFTER TIMEOUT MUTE

	LEFT CHANNEL								RIGHT CHANNEL							
	QUALDISL								QUALDISR							
ADDR.:	80	40	20	10	08	04	02	01	01	02	04	08	10	20	40	80
COLOR:	RD	RD	YL	YL	GN	GN	GN	GN	GN	GN	GN	GN	YL	YL	RD	RD
ABBR.:	ND	M	INT 1	INT 2	TL	FP	QP2 OK		QP2 OK		FP	TL	INT 2	INT 1	M	ND

The higher order bits are priority encoded by the system controller. The signal quality display in the tape deck is identical to that in the Display panel. Both are enabled/disabled with function 049 in the menu.

- five illuminated segments below the signal quality display indicate the display status of the seven segment LED display. The light bars show HEADROOM, GAINS, PEAK and CH 1 dB and CH 2 dB.

- the seven-segment LED display with 10 characters shows either one of the time functions, a digital or analog gain value in [dB], the peak value of the signal in [dB], or the headroom setting [dB].

The keyboard: 14 electronic keys with momentary contacts and associated LED's are provided. They are separated in two functional blocks. The block to the right consists of four keys, mainly for time display purposes. The left block serves level and gain display and setting purposes.
An external display panel can be connected to the rear of the tape deck (connector "Display panel"). **Do not connect an external display panel under power!**

Remote Display Panel:
A remote Display panel with 15m ribbon cable would be the device with the longest distance to the system controller. It may be necessary to remove the termination resistors in both Channel Control panel (jumper selectable) and internal Display panel. Insert jumper 1 (IC12, pin 9 tied to logical low level) to indicate to the system controller that two identical devices or just one single remote panel is connected. The command and status information is transmitted to both panels simultaneously from the system controller. The system controller acts on the last detected command from one of the panels.

TIME
Ring key for display of three different time functions:
- timer (no prefix) shows time derived from the move roller
- time code (prefix t) shows timecode (code, user bits or unassigned bits as selected with functions 407...411 in the menu) from the dedicated time code track (auxiliary track 1) or from an external generator in INPUT mode
- reference time (prefix r) shows internal reference time recorded on the reference time track (auxiliary track 2).

The functions may be activated by repeatedly pressing TIME for display in the seven-segement LED display.

RESET
Resets timer and/or reference time (not time code), depending on the display status to zero.
It also resets the error counters in accumulated error display mode (see section 2 of volume III of the D820X manuals).

WATCH
pressing the key selects WATCH mode for the seven-segment LED display, lead by prefix "I". The display may be set to zero with the RESET key or either stopped or started with the STOP key. This display mode is automatically selected when accumulated errors are displayed (show quality counters via terminal mode, described in section 2 of volume III of the D820X manuals). Note that accumulated errors is active only as long as the display is in WATCH mode.

START/STOP
Used in conjunction with WATCH for relative time measurements, or to START and STOP accumulating tape errors in "show quality" mode from terminal or personal computer only (see D820X manual, Vol. III, sect. 2) to assess the performance of the digitalaudio electronics or of the tape. The key located in the Display panel is used also to enable CAL GAINS, UNCAL GAINS, HEADROOM and PEAK mode, when pressed simultaneously with the desired key.

PEAK
It selects PEAK mode display of a source as selected with the INPUT and REPRO keys of the Channel Control panel. The peak value is indicated in dB relative to full scale (0 dBr). The last peak value is accumulated and displayed (peak hold mode). At the same time the letters "PEAK", "CH 1 dB" and "CH 2 dB" are illuminated. The peak hold memory is erased and set to - 60.4 dB when the RESET key is pressed and no signal for measurement is applied.
The peak level display in dBr is a convenient feature to adjust the headroom of the recorder, or its clipping level. The function may also be used for analog or digital tape or disk mastering applications.

GAIN AND LEVEL ADJUSTMENTS
The gains modes: three different gain sets are available for adjustment, storage and activation

- CAL GAINS (calibrated gains = default gain settings, analog + digital)
- UNCAL GAINS (uncalibrated gains = a second gain set, analog + digital)
- HEADROOM (the analog input and output gains are adjusted in inverse manner, the digital gains are not affected)

The analog gains are referred to absolute voltage levels relative to 0.775 V in [dBV.7]; the adjustable range is 4...24 dBV.7 and the resolution 0.1 dB.
The digital gains are referred to relative levels (to the 0 dBr digital level which corresponds to an amplification factor one), with an adjustable range from + 6 to -10 dB. The resolution is 0.1 dB. The analog and digital gains are connected in tandem for in- and output in the reproduce path; in the INPUT mode, the digital input gains are bypassed (see Fig. nnn).

CAL GAINS and UNCAL GAINS setting from remotes (RS-232, ES, terminal, etc.): only the specific gain set indicated in the display of the recorder is actually changed and its corresponding levels altered. The other gain set may be changed without really affecting the levels of the recorder (preparation mode). Those levels will be changed as soon as the corresponding gain set is selected on the recorder.

CAL GAINS

The keys CAL GAINS and STOP simultaneously pressed activate calibrated gain mode. The absolute voltage levels in [dBV.7] of the analog gains or the relative levels [re 0 dBr digital) of the digital gains are indicated on the seven-segment LED display. The indicated mode corresponds to the key settings "INPUT/OUTPUT", "ANALOG/DIGITAL" and "CH 1 dB" and "CH 2 dB". The label "GAINS" is illuminated. CAL GAINS can not be adjusted from the display panel. Functions 001...008 in the menu or the "clip level" or "digital gain" set functions of the alignment menu are to be used for this procedure. Switchover from all other gain modes is possible without click noises as long as consecutive settings are equal.
At power-up always calibrated gains are selected, also after disconnection of the display panel (volatile memory).
Press PEAK, TIME or WATCH to exit from calibrated gain level display, but not from calibrated gain status. For this, UNCAL GAINS or HEADROOM is to be selected, together with STOP. It will indicate the gain settings and activate a gain set which may be different!

UNCAL GAINS

The uncalibrated gains is an independent gain set for digital and analog gains. These gains are entered via display panel exclusively. Press key UNCAL GAINS together with STOP to activate uncalibrated gains. The absolute voltage levels in [dBV.7] for the analog gains or the relative levels [re 0 dBr digital] for the digital gains are indicated on the seven-segment LED display. The indicated mode corresponds to the key settings "INPUT/OUTPUT", "ANALOG/DIGITAL" and "CH 1 dB" and "CH 2 dB". The label "GAINS" is illuminated. The yellow LED in the key UNCAL GAINS is flashing as long as this mode is active. The indicated gain settings may be altered in the range 4...24 dBV.7 for analog levels and + 6...- 10 dBr for digital gains in 0.1 dB steps.
The entire CAL GAINS memory may be copyed into UNCAL GAINS memory by pressing the keys CAL GAINS and UNCAL GAINS together for approximately 1 second.

HEADROOM

Description of headroom mode:

- it inverses the indication of the level display section
- the analog in- and output levels are adjusted such that, e.g., when positive headroom is ajusted, the analog input will be less sensitive (input level increased) and the analog output level is increased, yielding a balanced overall level adjustment for the recorder.

Procedure to adjust the headroom of the recorder:

- copy the desired gain set into headroom memory: press CAL GAINS or UNCAL GAINS together with HEADROOM. This duplicates the calibrated gains or the uncalibrated gains into headroom memory and activates headroom mode. By this procedure, the 0 dB reference for headroom is set, from which headroom can be adjusted. It allows also to enter headroom mode without any clicks, because no gain change has taken place. Headroom mode activation is indicated by a flashing yellow LED in key HEADROOM.
- select headroom level (positive or negative) with UP and DOWN keys in 0.5 dB steps. Max. range is ± 5 dB. When e.g. + 1.5 dB headroom is selected, the analog input and output levels are increased by 1.5 dB. The maximum level range of the recorder (4...24 dBV.7) can not be exceeded. The relative headroom is indicated in [dB] for both channels in the LED display.
- to exit from headroom mode: press TIME, WATCH or PEAK.
- to reenter headroom mode: press HEADROOM together with STOP.

After power-up the default values for the headroom memory are loaded. Make sure to use the appropriate level set (CAL GAIN set or UNCAL GAIN set) by copying the desired set into headroom memory (see par. a above).

CH 1 dB
Shows the value of the gains or levels for CH 1 in the LED display. Adjustment of gains is possible only as long as the label "CH 1 dB" is illuminated, but the value is always displayed for reference purposes.

CH 2 dB
Shows the value of the gains or levels for CH 2 in the LED display. Adjustment of gains is possible only as long as the label "CH 2 dB" is illuminated, but the value is always displayed for reference purposes.

ANALOG/DIGITAL
Shows and/or activates the corresponding gains of the selected gain set (calibrated gains or uncalibrated gains) in CAL GAINS or UNCAL GAINS mode only.

INPUT/OUTPUT
Shows and/or activates the correspoinding gains for analog or digital input or output of the selected gain set (calibrated gains or uncalibrated gains) in CAL GAINS or UNCAL GAINS mode only.

UP/DOWN
De- or increment gains and/or levels. Two modes: single step (when pressed intermittently), or continously (when the button is held down for some time).

2.5.23 Monitor Panel (Version -2PPM)

TAPE and CH1 and/or CH2
Monitoring of the main (digitalaudio) channels 1 and/or 2 in reproduce or record mode is selected, depending on whether keys CH1 or CH2 or both are pressed. When only one channel is selected, both speakers are fed with identical signals. Keys CH1 and CH2 interlock against CUE1, CUE2 or MIX, AUX.
The routing is provided from the Analog Output board directly to the input of the Analog Routing board for good audible quality.

INPUT and CH1 and/or CH2
It may be performed in all tape deck modes. Either the analog or the digital main input is selected, according to key 018: INPUT: DIGITAL/ANALOG. The signal is routed from the Data Processor (DAPRO) via EEPDM (modulator-demodulator) to the Analog Routing board. The audio quality is slightly impaired due to the EEPDM loop, noticeable especially with high level test signals.

TAPE and CUE1 and/or CUE2 or MIX or AUX
Off-tape monitoring of the cue tracks or of the dedicated data track, selection according to key 044 ASSIGN AUX3: DATA/CUE. When this key is in position "cue", stereo playback of the cue tracks is enabled. Track selection with keys CUE1 and/or CUE2. When only one channel is selected, both speakers are fed with identical signals. Keys CUE1 and CUE2 or MIX and AUX interlock against CH1 and CH2.
When key 044 is in position "data", a mixture of both main (digitalaudio) tracks is performed on the PDM Modulator board. This sum signal can be monitored when key MIX is pressed. Key AUX selects data track auxiliary 3 (check function only).

Constraint: only the last update is written on tape after single track recordings or single track overdubs. There is no mix of previously recorded information with new recordings.

INPUT and CUE1 and/or CUE2 or MIX or AUX
Monitoring of the input of the cue tracks or of the dedicated data track. Otherwise see paragraph above.

TC

TC is a momentary key which overrides all other functions. When pressed, the off-tape TC track becomes audible on both speakers. The signal is derived from the output of the Playback Amplifier board.

AUTOEDIT

Function 017 AUTOEDIT activated affects the monitor speakers and automatically switches to playback of the main (digitalaudio) channels in PLAY and REC mode, else (in STOP, EDIT, WIND, LOC, TAPE DUMP) the cue tracks are selected. Overriding of the key settings on the Monitor panel is possible everytime. The AUTOEDIT status is restored by pressing STOP.

MUTING OF MONITOR SPEAKERS

Both speakers with the exception of the headphone output are muted when fader start is active (see par. 2.5.15), or when a headphone connector is inserted into the "phones" socket.

2.5.24 Editing, Tape Splicing

Searching a tape location with spooling: if the desired tape address is approximatively known (e.g. the beginning or the end of a selection), it can be approached with the spooling function. Press the programmable LIFTER key so that the tape lift pin is pushed behind the heads in order to position the tape by monitoring the cue tracks. As soon as the cue point is reached, the tape can be fine positioned by repeatedly pressing ◄ and ►, by actuating the SHUTTLE wheel or by pressing EDIT and turning the SET/CUE wheel. Press STOP and bring the tape in the exact splicing position by carefully rotating one of the two reel flanges by hand.

Search with PLAY: if certain segments with unknown locations are to be cut out of a program, they can be searched in normal PLAY mode. When one of these segments has been located, press the STOP key and position the tape into the correct cutting position by carefully rotating one of the two reel flanges by hand.

Search with autolocator: the tape address 0.00.000 can be automatically located with the ZERO LOC function. The start of a sequence is programmatically stored in memory and can be automatically retrieved with the LOC START key if the recording or playback has been uninterrupted.

While a program is being recorded or reproduced, up to 5 tape addresses can be stored directly, depending on the programming of the recorder, by pressing TRANS and LOC1 (...5) in the desired tape position. When the corresponding LOC button is pressed, the desired tape address is automatically located; the exact editing position can now be adjusted manually.

Cutting with built-in tape scissors: pressing the (programmable) CUT key positions the tape automatically in front of the built-in scissors. The tape is cut by pressing the button over the scissors. By pressing the TAPE DUMP key a segment of tape that is to be discarded can be played into the waste basket (see 2.5.25, TAPE DUMP mode).

Marking the tape, cutting in splicing block: mark the tape in front of the center of the reproduce head (right hand side) with a very soft pencil, a fluorescent felt pen (different colors are available) or a video marking pen. Grease pencils are not recommended because they normally destroy areas on the front coating of the next layer due to printing.
The marked position is placed into the splicing block (in front of the headblock) and cut with a razor blade perpendicular to the tape edge.

Splicing the tape: place the two tape segments with the marked side facing upward into the splicing block. Butt the two ends together by leaving a small gap of approximately 0.1 mm (overlapping is not permitted!) and secure it with an approximately 20 mm long and less than 1/4" wide piece of adhesive tape. This adhesive tape should be as thin and as flexible as possible in order not to cause distance losses when the ends of the splicing tape pass the heads (maximal thickness of 27 micrometer). Recommended types are listed in par. 1.5. Make sure that both surfaces of the splicing tape and the splicing block itself are absolutely clean, in order not to damage the coating of the tape (visual inspection of the splicing area after applying the splicing tape is recommended). Check the position of the splicing tape. It must not protrude the tape. This would cause azimuth errors.

Please refer to section 2.8.1 for a more thorough treatment of the tape cutting process.

2.5.25 Tape Dump

In dump edit mode the right-hand spooling motor is switched off. Unwanted tape segments can be played into the waste basket by activating this mode.
When the TAPE DUMP key is pressed, the recorder switches either to PLAY, or TAPE DUMP mode as preselected - see below. The right-hand spooling motor remains switched off.
The main (digitalaudio) channels are muted during this mode. The cue channels are active, but the tape speed does not exactly correspond to one of the nominal speeds, selected by the sampling frequency key.
Four TAPE DUMP versions are available:

- TAPE DUMP A: tape counter active, function to be canceled with STOP or by pressing TAPE DUMP again.
- TAPE DUMP B: same as TAPE DUMP A, however the tape counter is blocked.
- TAPE DUMP C: pressing TAPE DUMP preselects dump edit mode; activation by pressing PLAY, interruption only in STOP mode, by pressing TAPE DUMP again.
- TAPE DUMP D: same as TAPE DUMP C, however the tape counter is blocked.

Winding up a loose piece of tape: in the event that too much tape is played into the waste basket in tape dump mode it is not necessary to laboriously rewind the tape by hand. Simply thread the tape (or let it be threaded) as illustrated in Fig. 2.5.11 and carefully tension the loose tape end with two fingers, but insert a soft tissue between fingers and tape to avoid fingerprints and do not expect an improvement of the block error rate due to crude tape handling. Keep the rewind key pressed: the left-hand (supply) reel turns clockwise and rewinds the tape. This operation can be canceled by releasing the REWIND key. Make sure that the tape has not been damaged by the entire operation!

The torque of the motor is limited and controlled in such a way that the tape can be easily braked by hand. If you let loose of the tape end, the motor turns very slowly. Its speed can be increased by lightly pulling on the tape.
The same applies analogously to winding a piece of tape with the right-hand (take-up) motor. The only thing that is important is that the tape segment to be wound is threaded around the tape tension sensor and its adjacent guide rollers to ensure that the tape tension control loop can function correctly.
Playing a dumped tape segment: after some editing work it may happen that many individual tape segments have been dumped into the waste basket but the operator is not sure whether or not they contain any usable audio material. Such tape sections may be played with the D820X without having to be spliced first and wound onto a reel (cue tracks and time code track only).
Procedure: press EDIT button, the tape transport and the pinch roller start up. The EDIT button turns on, STOP flashes. Thread the tape segment according to Fig. 2.5.12.

With your left hand lightly tension the tape segment on the lefthand side of the headblock. The tape is cued by running over the reproduce head (cue tracks and time code only). If a small amount of backtension is produced with the left hand, the contact between tape and head is improved (better reproduction). The tape may have to be cleaned from possible dust particles that have been picked up in the waste basket. Fingerprints will certainly degrade the signal quality of the main channels.
Pressing EDIT interrupts the procedure. To cancel the function press STOP.

2.5.26 Varispeed

With the built-in varispeed control the nominal tape speed can be varied by ± 7.5 semitones (± 12.5 %).
The speed change can be preselected with the SET VARISP key and the SET/CUE wheel (the latter functions as a potentiometer), without influencing the current nominal speed. The preselected speed is indicated on the service display, depending on the programming, either in semitones, in percent of the nominal speed, or as the actual tape speed value in inches per second (ips).
The VARISPEED button is pressed to switch from the nominal speed to the changed speed - the VARISPEED lamp above the tape counter flashes.

If the functions SET VARISP and VARISPEED are active at the same time, the speed change is implemented immediately (with the SET/CUE wheel). The result can be heard directly during playback.
Here some notes on the varispeed operation of a digital recorder: varispeed is enabled in all transport modes, except in digital input mode, or with wordclock sync, or when set to accept a signal applied to pins SR-VRSPD of the parallel synchronizer and remote control ports (in SYNCHRONIZER ON mode or when function 058, SYNC IN SYNCHR is active). The message "digital input sync mismatch" appears in the service (LCD) display. In the control word of the digital output (DO), bit 5 of byte 00 is set high when varispeed is selected. In all these modes, a phaselock of the entire recorder (in- to output) is required to preserve the blocking structure. The delay time from in- to output is then constant. These requirements can not be matched in varispeed mode. In order to transfer digital data from a source with different sampling frequency a sampling frequency converter is necessary (e.g. STUDER SFC 16).

Note: Valid digital transfer between equipment is specified for 3 sampling frequencies (48, 44.1 and 32 kHz) with deviations of ± 10 ppm, according to the AES/EBU and ANSI standard (see interfacing specifications). the sampling frequency 44.056 kHz can not be specified in the control word of the source directly. Transferring is possible by setting bits 6 and 7 of byte 0 of the control word to low (unspecified). It is mandatory to observe the same frequency tolerances as above.

2.5.27 Displays

The D820X contains an LED display on its transport and on some remote devices for time display and (on the Display panel) for level display in [dB]. Refer to par. 2.5.13 (time) or 2.5.22 (Display panel).
The tape deck also exhibits a service (LCD) display for entering and display of menu and error functions. It is used when soft keys are to be reassigned (par. 2.6, examples), to display tape deck settings (tape tension, etc.) and to set wind speeds, serial port parameters and line levels.
Sixteen colored LED's are located on top of the LCD display of the tape deck and on top of the Display panel. They can be activated/desactivated with key 049 QUALITY DISPLAY and show signal quality of the main (digitalaudio) channels in PLAY and REC mode according to the table below.

Composition of Signal Quality Data

ORIGIN	ADDR	NAME	ABBREV	DESCRIPTION
SYSCON	01	LOW ERROR RATE	OK	NORMAL BEHAVIOR
CODEC	02	QP2 CORRECTION	QP2	SECOND PASS QP-PARITY CORRECTION
CODEC	04	FINGERPRINT	FP	FINGERPRINT ≥4 TRKS, T<<
CODEC	08	TRACKLOSS	TL	≥1 TRK, T≥512 BLOCKS (1/4 SEC.)
DAPRO	10	INTERPOLATION 2	INT 2	INTERPOLAT. 2ND GRADE (QUADRATIC)
DAPRO	20	INTERPOLATION 1	INT 1	INTERPOLAT. 1ST GRADE (LINEAR)
DAPRO	40	MUTE	M)	MUTE WITH TIMEOUT 0.5 SEC.
SYSCON	80	NO DATA	ND)	AFTER TIMEOUT MUTE

	LEFT CHANNEL								RIGHT CHANNEL							
	QUALDISL								QUALDISR							
ADDR.:	80	40	20	10	08	04	02	01	01	02	04	08	10	20	40	80
COLOR:	RD	RD	YL	YL	GN	GN	GN	GN	GN	GN	GN	GN	YL	YL	RD	RD
ABBR.:	ND	M	INT 1	INT 2	TL	FP	QP2 OK		QP2 OK		FP	TL	INT 2	INT 1	M	ND

The higher order bits are priority encoded by the system controller.
The service keyboard also features pilot lamps to indicate the status of several functions. Most of the LED's are self-explanatory, the lamps for the sampling frequency, however, require special attention. They turn on only when the recorder has been able to achieve locking to the desired sampling rate. Several conditions must be fulfilled in digital input mode (see key 018 INPUT: DIGITAL/ANALOG).
The four red LED's are flashing when activated because they indicate operational modes for which special considerations are required.
More displays are obtained by connecting terminals or computers to the "test" connector at the PCM box or to the serial remote port of the transport. Refer to par. 2.10 for operation with the serial interface or to vol. III of the D820X manuals for instructions on the Master Monitor and the Syscon Monitor.

2.6
Soft Keys

Except for the four blue keys and the red "store" key of the function and programming key field below the hinged cover, all operating keys of the D820X digital tape recorder can be assigned to any of some 150 functions or operating modes.
It is also possible to enter certain operating modes (subsequently designated as K/M or KEYS/MODE) directly, or to change them without assigning any of the operating keys to them.
This function assignment procedure is simplified by the service display (alphanumeric LC display, on the right front of the tape transport) as well as by the top-down tree structure diagram illustrated on the page "menu structure and functions".

This diagram consists of

blocks

and setting positions.

After the recorder has been switched on, the first four (or possibly five) blocks appear consecutively on the service display for a few seconds each:

D820X SOFTWARE VERS: MASTER: WW/YY

Creation date of the software of the MASTER MPU, calendar week/year.

Possible error messages resulting from the automatic test, either in plain text or the message "no errors detected", or loading of default parameters (i.e. after RAM errors, etc.) are displayed in the error message window (see below).

ERROR MESSAGE

LEVEL A:xx.x D: xx.x FR/SEC xx DELAY xxx

The analog line (clipping) level of the recorder, calibrated in dBV.7 (or dBu), and the digital levels in dB relative are indicated in the top row. The analog levels represent maximum values just at the verge of clipping. No extra headroom is provided (see par. 2.6.4 below, section "clip levels", for more information on this topic). If the levels for both channels and for in- and output are not set to the same numerical value, --- is displayed in the appropriate field.
The frames per second (FR/SEC) indication shows the frame rate selected for time code, either 25, 29.97 or 30 frames. Only the first two numbers are indicated (25/29/30). The second item in the lower line shows whether the time code output delay is active or not. Both functions can be found in the time code menu.
The sequence stops here. In normal operating mode, the above four blocks can be retrieved by pressing /LAST.
Other information is only displayed when the programming key field is actuated, provided programming has been enabled with switch [28] (Allen screwdriver No. 2.5; clockwise limit position = programming disabled, counterclockwise limit position = programming enabled.
Reprogramming of the keys is not possible when the switch is in the disable position; should any attempt be made, the message "program mode not enabled" appears on the display.

With the keys ↓/NEXT, ←/CURSOR, →/CURSOR, and ↓/LAST it is possible to move up and down in the alinment menu and to the headers of the mode menu, where the cue wheel has to be used to proceede within columns. In branching points the cursor is to be positioned under the desired menu.

2.6.1 Menu Structure and Functions

2.6.1.1 Alignment Menu

It consists of two columns: audio and deck. Move up and down with NEXT and LAST keys. Change settings with the cue wheel. Store the desired adjustment with the STORE key (exceptions: RECORD CURRENT A and B, REFERENCE EQ TABLE and STOP ADAPTATION: press STORE and RECORD).
Some of the positions require the **cue wheel** to gain access to submenus:

REFERENCE EQ TABLE: "selected", "not selected"
STOP ADAPTATION: "selected", "not selected"

HUB DIAMETER: "NAB", "DIN", "DIN A", "CINE A", "CINE B", "CINE C"

BINARY RS-232/422 FORMAT: "8 bit, 2 stopbits", "8 bits, 1 stopbit", "8 bits, even parity, 1 stopbit", "8 bits, odd parity, 1 sb"

Some of the functions require **REC and STORE** pressed simultaneously for activation: REFERENCE EQ TABLE, STOP ADAPTATION and entering different settings for RECORD CURRENT A or B.

Remark on Reference Table and Stop Adaptation:
The D820X uses a propretary adaptive digital playback "equalization" method. With the REFERENCE EQ TABLE function, the adaption process is disabled when selected. Equalization is then derived from a ROM table which has been programmed using standard head, tape and read electronics. The block error rate may increase. Greater deviations from the values obtained in the factory (see specifications) should give rise to further inspections of the head-tape environment, provided that the tape specifications are within close limits.

The STOP ADAPTATION function freezes the last content of the RAM's of the Adaptive Run Processor. Their content normally adopts to the varying head-tape conditions.

2.6.2 Numbering of the Keys

The operating keyboard is designed as a matrix consisting of five rows of up to ten keys.

Numbering:

2.6.3
Available Functions

Version A: D820X-2 (w/o Channel Control, Display and Monitor panels)
Version B: D820X-2PPM (with panels)

Normally the parameter to the far right side of certain keys is the default value.

AUDIO

No.	Function	Typ	No. of key at version A	B
001	CLIP LEVEL 4dBm Y/N	K/M	---	---
002	CLIP LEVEL 6dBm Y/N	K/M	---	---
003	CLIP LEVEL 8dBm Y/N	K/M	---	---
004	CLIP LEVEL 10dBm Y/N	K/M	---	---
005	CLIP LEVEL 15dBm Y/N	K/M	---	---
006	CLIP LEVEL 20dBm Y/N	K/M	---	---
007	CLIP LEVEL 24dBm Y/N	K/M	---	---
008	DIGITAL GAIN 0dB Y/N	K/M	---	---
010	INPUT Y/N	K/M	---	---
011	REPRO Y/N	K/M	---	---
014	AUTOINPUT A: Y/N	K/M	---	---
015	AUTOINPUT B: Y/N	K/M	---	27
016	AUTOMUTE: ON/OFF	K/M	---	---
017	AUTOEDIT: ON/OFF	K/M	---	26
018	INPUT: DIGITAL/ANALOG	K/M	37	37
019	EMPHASIS: ON/OFF	K/M	34	34
020	SAMPLING RATE: LO/HI	K/M	33	33
021	SAMPLING RATE HI: Y/N	K/M	---	---
022	SAMPLING RATE LO: Y/N	K/M	---	---
023	SYNCHRONIZER ON/OFF	K/M	---	---
025	CH CONTR.: PAR/INDIV	K/M	---	---
030	CHANNEL 1: SAFE/READY	K/M	---	---
033	CHANNEL 2: SAFE/READY	K/M	---	---
036	TIMECODE: SAFE/READY	K/M	27	---
039	RT SYNC: ON/OFF	K/M	26	---
042	AUX 3: SAFE /READY	K/M	---	---
043	MASTERSAFE: ON/OFF	K/M	36	36
044	ASSIGN AUX3: DATA/CUE	K/M	---	---
045	AUX3+4: MANUAL/AUTO	K/M	---	---
046	CUE: UNMODULATED/AUTO	K/M	---	---
047	CUE: MODULATED/AUTO	K/M	---	---
048	HI PASS FIL: ON/OFF	K/M	---	---
049	QUALITY DISP: ON/OFF	K/M	---	---
050	LEVEL DISP: NORM/INPT	K/M	---	---
051	SYNC IN: EXT/INT	K/M	35	35
052	SYNC IN: BAL/UNBAL	K/M	---	---
053	SYNC IN WORD CLK: Y/N	K/M	---	---
054	SYNC IN DIG INPT: Y/N	K/M	---	---
055	SYNC IN VID EBU: Y/N	K/M	---	---
056	SYNC IN NTSC B/W: Y/N	K/M	---	---
057	SYNC IN NTSC COL: Y/N	K/M	---	---
058	SYNC IN SYNCHR: Y/N	K/M	---	---
059	SYNCOUT SECT CLK: Y/N	K/M	---	---
060	SYNCOUT WORD CLK: Y/N	K/M	---	---
064	IGNORE DI C WORD: Y/N	K/M	---	---
065	MASTERING ON Y/N	K/M	---	---
070	TEST ON/OFF	K/M	---	---
101	REHEARSE	K	---	---

TAPE DECK

201	TAPE GUARD A: RED/NO	K/M	---	---
202	TAPE GUARD B: STOP/NO	K/M	---	---
210	VARISPEED %: Y/N	K/M	---	---
211	VARISPEED HT: Y/N	K/M	---	---
212	VARISPEED IPS: Y/N	K/M	---	---
213	VARISPEED: %/IPS/HT	K/M	---	---
214	VS IND ENHANCED: Y/N	K/M	---	---
220	FADER START A: Y/N	K/M	---	---
221	FADER START B: Y/N	K/M	23	23
222	FADER START C: Y/N	K/M	---	---
223	FADER START D: Y/N	K/M	---	---
301	REWIND	K	07	07
302	FORWARD	K	06	06
303	LIBRARY WIND	K	13	13
304	PLAY	K	05	05
306	STOP	K	04	04
307	RECORD A	K	03	03
308	RECORD B	K	---	---
309	EDIT	K	02	02
310	CUT	K	12	12
311	TRANSFER	K	17	17
312	HOLD	K	---	---
313	LOCATOR 1	K	16	16
314	LOCATOR 2	K	---	---
315	LOCATOR 3	K	---	---
316	LOCATOR 4	K	---	---
317	LOCATOR 5	K	---	---
318	ZERO LOCATOR	K	15	15
319	LOC START STOP	K	---	---
320	LOC START PLAY	K	14	14
321	LOC START REC	K	---	---
322	ROLLBACK STOP	K	---	---
323	ROLLBACK PLAY	K	---	---
324	ROLLBACK REC	K	---	---
327	TAPE DUMP A	K	11	11
328	TAPE DUMP B	K	---	---
329	TAPE DUMP C	K	---	---
330	TAPE DUMP D	K	---	---
332	LIFTER	K	---	---
334	START/STOP	K	---	---
335	RESET TIMER	K	41	41
336	SET TIMER	K	---	---
337	SET ADDRESS	K	---	---
338	SET VARISPEED	K	24	24
339	VARISPEED ON/OFF	K	25	25
345	REMOTE A	K	---	---
346	REMOTE B	K	---	---
347	SHUTTLE BAR	K	01	01
355	TIME DISPLAY	K	---	---
356	WATCH DISPLAY	K	---	---
357	RT DISPLAY	K	---	---
358	TIMECODE DISPLAY	K	---	---
359	TIME/WATCH DISPLAY	K	---	---
360	TIME/WATCH/RT/TC DIS	K	40	40
361	UNLOAD	K	10	10
362	NO FUNCTION	K	---	---

TIME CODE

401	25 F/SEC: Y/N	K/M	---	---
402	29.97 F/SEC: Y/N	K/M	---	---
403	30 F/SEC: Y/N	K/M	---	---
404	25/29.97/30 F/SEC	K/M	---	---
405	25/29.97 F/SEC	K/M	---	---
406	29.97/30 F/SEC	K/M	---	---
407	DISPLAY CODE: Y/N	K/M	---	---
408	DISP. USER BITS: Y/N	K/M	---	---
409	DISP. UNASS. BITS:Y/N	K/M	---	---
410	DISPLAY USER/CODE	K/M	---	---
411	CODE/USER/UNASSIGNED	K/M	---	---
415	TC: UNMODULATED/AUTO	K/M	---	---
416	TC: MODULATED/AUTO	K/M	---	---
425	TC DELAY: OFF/AUTO	K/M	---	---
426	TC DELAY: ON/AUTO	K/M	---	---
501	FOR FUTURE USE ONLY	K	---	---

2.6.4
Description of Functions

CLIP LEVEL 4dBm (No. 001) KEYS/MODE
CLIP LEVEL 6dBm (No. 002) KEYS/MODE
CLIP LEVEL 8dBm (No. 003) KEYS/MODE
CLIP LEVEL 10dBm (No. 004) KEYS/MODE
CLIP LEVEL 15dBm (No. 005) KEYS/MODE
CLIP LEVEL 20dBm (No. 006) KEYS/MODE
CLIP LEVEL 24dBm (No. 007) KEYS/MODE

Seven preset clippping levels are available. Any other level between 4 and 24 dBV.7 (dBu) can be adjusted when the corresponding function in the alignment menu is utilized. With a pre-set level out of this selection, both analog input and output levels are set to the same value and are indicated in the LC-display.
These levels are referred to as "calibrated gains" and can be changed only from the recorder or remote devices, in comparison to the "uncalibrated gains", which are accessible from the display panel. The "calibrated gain" set is normally used in the studio, whereas the other can be helpful in the field, e.g. for operation with different clipping levels.
A short explanation on the term "clipping level": it defines the maximum analog in- or output level of the recorder. When the input level is increased, the analog-to-digital converter clipps the signal (hard clipping). The indicated output level is obtained, when a full scale analog or digital input signal is applied.
There is no implicit headroom provided with a level out of this selection. The amount of headroom is subject to personal opinion (whether occasional clippings can be tolerated or not) and to the hardware periphery of the recorder, namely the level metering in use. With VU-meters, approximately 10 to 20 dB headroom may be required, depending on the habit of the sound engineer. With quasipeak program meters and their much faster response, 3 to 10 dB may be sufficient. Adjust the clippping level of the recorder by the amount of headroom required above the line level of the peripheral hardware. When true peak metering is in use throughout the studio, no headroom is required at all and the line level of the studio can be identical to the clippping level of the recorder.
The unit [dBm] is not strictly correct, since power matching is no longer in use in recording studios. Any absolute voltage level referenced to 0.775 Volt is meant here. The term [dBm] is used for convenience.
Factory default setting for analog in- and output levels is 15 dBm.

More information on gain, headroom, level and metering functions can be found in section 2.5.22 Display Panel.

The "show gains" diagnostic screen indicates calibrated gains, uncalibrated gains and headroom settings at one glance (terminal or personal computer connected to the "test" connector).

DIGITAL GAIN 0dB (No. 008) KEYS/MODE

The digital gains are relative levels referenced to 0 dB. The adjustable range is +6...-10 dB (from the alignment audio menu only). The digital in- and output gains are set to 0 dB gain (amplification factor 1) when the function above is activated.
The resolution is 0.1 dB. The analog and digital gains are connected in tandem, except in INPUT and local REHEARSE mode, where the digital output gains are bypassed.
Factory default setting for digital gains is 0 dB.

More information on gain, headroom, level and metering functions can be found in section 2.5.22 Display Panel.

The "show gains" diagnostic screen indicates calibrated gains, uncalibrated gains and headroom settings at one glance (terminal or personal computer connected to the "test" connector).

INPUT Y/N (No. 010) KEYS/MODE

This function connects the analog or digital input to the outputs for monitoring and metering purposes of the main channels. The digital output gains are bypassed when INPUT is selected. INPUT-keys for the auxiliary data track 3 and for time code are provided on the Display Panel. Single channel operation is possible, depending on the setting of function 25, CHANNEL CONTROL: PARALLEL/INDIVIDUAL. Overriding is performed with the keys of the Channel Control panel.

Similar functions as INPUT are AUTOINPUT A and B, described below.
ON/OFF key. Default: INPUT off.

REPRO Y/N (No. 011) KEYS/MODE

With REPRO on, off-tape monitoring and metering of the main channels is selected. Single channel operation is possible, depending on the setting of function 25, CHANNEL CONTROL: PARALLEL/INDIVIDUAL. Overriding is performed with the keys of the Channel Control panel.
More on reproduce can be found in chapter 2.5.6.
ON/OFF key. Default: REPRO on.

AUTOINPUT A: Y/N (No. 014) KEYS/MODE AUTOINPUT B: Y/N (No. 015) KEYS/MODE

All channels (in AUTOINPUT A) or all channels in READY status (AUTOINPUT B) are set to INPUT in operating modes STOP, REWIND, FORWARD, LOC and ROLLBACK. In both modes, overriding is performed by means of the keys of the Channel Control panel (CCP) and Monitor panel (MP). Only digitalaudio channels are controlled by the AUTOINPUT functions.
ON/OFF keys. Default: AUTOINPUT B.

AUTOMUTE ON/OFF (No. 016) KEYS/MODE

Automatic muting in spooling mode and during the start-up phase (until nominal speed is attained) for cue outputs AUX 3 and AUX 4.
ON/OFF key. Default: OFF.

AUTOEDIT ON/OFF (No. 017) KEYS/MODE

When activated: the internal monitor reproduces the main tracks (digitalaudio) in PLAY mode. The internal monitor reproduces the cue track(s) in STOP, EDIT, WIND and TAPE DUMP mode. Overriding of the function is possible with the keys of the Monitor panel (MP) in all modes. The initial status is restored by pressing the STOP key.
When not active: the internal monitor reproduces the cue tracks in all tape deck modes. Overriding by the keys of the Monitor panel (MP) is possible. The initial status will not be restored.
ON/OFF key. Default: OFF.

INPUT: DIGITAL/ANALOG (No. 018) KEYS/MODE

When DIGITAL input is active, the recorder is by definition in slave operation. The master is the first device of the digital link. Check the yellow pilot lamp on top of the secondary keyboard. It is illuminated when incoming and local sampling frequencies match, when the crystal configuration of the recorder is correct and when byte 0 of the control word is appropriately set. Otherwise, the recorder can not lock to the source. More information can be found on the LC-display (i.e. error message "DI unlock") and on the status diagnostic screen, when a terminal or personal computer is connected to the recorder (see "error"-line: DI out-of-lock, VCXO out-of-lock, etc.). The recorder locks to external sources with sampling frequency tolerances as indicated in chapter 1.7, interfacing specifications.
When DIGITAL input is choosen, no other external sync source is allowed. The digital input derives its synchronization signal out of the data stream.
The D820X principally supports the professional version of the serial digital input format, generally known as "AES/EBU" format, and processes byte 0 of the control word at its in- and output. The domestic version of this interface standard is followed in one respect only: the emphasis flag is processed. When not the professional version of the format is detected at the input, an error message "illegal di format" appears and the error-LED is flashing. Note that when such an error message is suppressed by activating key IGNORE DI C WORD, no automatic processing of either format takes place. The digital input control word has top priority in STOP, EDIT, INPUT or RECORD mode. Second priority is tape and third local or remote commands. An exception to this rule is only made in PLAY mode, where the EMPHASIS flag from tape is shifted to the highest hierarchical level. For more information on EMPHASIS control with digital input, see key EMPHASIS below.
Selecting the sampling frequency locally is disabled, when the control word carries an override disable flag. Note that the recorder no longer follows the content of the reference time control word regarding sampling frequency, when override disable is specified from the master. An erroneous tape speed may result and an error message "rt fs mismatch" appears in the service display. Refer to key SAMPLING RATE below for more information.
Varispeed operation is disabled in DIGITAL input mode.
When the analog input is selected, synchronization may be derived either locally or from a remote source.
Refer to key 64, IGNORE DI C WORD, when control via digital input is not desirable.
The status of byte 00 of the master of a digital link (or of any of the devices between master and slave) can be checked with the "show status" or "show rt" diagnostic

screens, when a terminal or computer is connected to the "test" connector at the PCM-box. Refer to vol. III of the D820X manuals for a detailed description (section Syscon Monitor).

DI CHANNEL STATUS DIAGNOSTICS

BYTE NO	SIG NAME	DESCRIPTION	MSB BITS	7	6	5	4	3	2	1	0
5 (58H)	DIEMPH	AUDIO CHANNEL STATUS BYTE 00		0	1	2	3	4	5	6	7

BYTE 00:
BIT 00 : 0 = CONSUMER / 1 = PROFESSIONAL USE
BIT 01 : 0 = NORMAL / 1 = NON-AUDIO
BITS 234: EMPHASIS (*)
BIT 05 : 0 = SOURCE FS LOCKED / 1 = SOURCE FS UNLOCKED
BITS 67 : SAMPLING FREQUENCY (**)

(*) 000 = emphasis not indicated, manual override enabled, default: off
100 = no emphasis, receiver manual override disabled
110 = 50/15 µsec. emphasis, receiver manual override disabled
111 = ccitt-emphasis, receiver manual override disabled

(**) 00 = samp. frequ. not indicated, manual override enabled, def.= 48 kHz
01 = samp. frequ. 48 kHz, manual override disabled
10 = samp. frequ. 44.1 kHz, manual override disabled
11 = samp. frequ. 32 kHz, manual override disabled
BIT 0: if set low, emphasis BIT 3 processed only
BIT 1: not considered in D820X.
BIT 5: if set HI: SEND /MAINMUTE/ to protect analog outputs and display error message type a, led "ERROR" flashing, led "EXT. SYNC" dark, message "DI UNLOCK".

Default: ANALOG.

EMPHASIS: ON/OFF (No. 019) KEYS/MODE

The DASH format specifies the use of one set of time constants (T1 = 15 and T2 = 50 microseconds), which can be activated by this key. Another set of time constants is specified in the professional version of the digital in- and output format (CCITT J17 time constants). The D820X, however, is not equipped accordingly. An error message will appear when forced into record mode with CCITT emphasis. The digital in- and output is transparent in STOP or INPUT mode (control word, bits 2...4, patterns 000 and 111).
There are two general cases after which EMPHASIS is controlled: digital input (DI) active or non-active. In non-active DI mode and in PLAY, EMPHASIS is set according to the information contained in the data blocks and the digital output (DO) control word is either set to 100 for no emphasis, receiver manual override disabled, or 110 for time constants 15 and 50 microseconds (emphasis on), receiver manual override disabled.
On the recorder, overriding of the off-tape EMPHASIS setting is possible either locally or remotely, with an appropriate error message in the LC-display indicating "tape emphasis mismatch" and a flashing error-LED as long as an erroneous condition exists.
EMPHASIS can be changed in STOP mode any time. In RECORD mode, overriding is disabled and the state of the key prior to the RECORD achieved status is recorded on tape and the hardware is configured accordingly.
With DI active: when the recorder is not in PLAY mode and override disable is specified from the input, the EMPHASIS setting can not be changed locally or from a remote device, except from the source of the digital transmission link, otherwise, with pattern 000, override is enabled. When pattern 111 is received, the output is transparent in STOP or INPUT mode and the recorder enables overriding (for trial) but displays a format mismatch message.
In PLAY mode, the recorder reacts to the information contained in the data blocks independent from override specifications transmitted by the source.
In RECORD mode, the recorder acts according to the control word of the digital input, except when override is enabled. Information from previously written data on tape is

ignored. When CCITT J17 emphasis is requested by the digital input, the recorder displays a format mismatch message and the error-LED is flashing.
There are several special conditions affecting EMPHASIS setting:

- EMPHASIS is handled strictly for stereo operation. When an attempt is made to override one single track with a different setting as previously written on tape, an "override disabled" message appears and the attempt is neglected.

- when the control word follows the consumer format, only one bit specifies the EMPHASIS setting. Therefore, override is disabled as soon as the control word of the consumer format is detected in order to eliminate operational errors.

Refer to key 018 above for DI channel status diagnostics.
ON/OFF key. Default: OFF.

SAMPLING RATE: LO/HI (No. 020) KEYS/MODE

SAMPLING RATE HI: Y/N (No. 021) KEYS/MODE

SAMPLING RATE LO: Y/N (No. 022) KEYS/MODE

The SAMPLING RATE keys select one of two installed sampling rates according to the crystal (VCXO) configuration of the recorder. The crystals are located on the VCXO board 1.861.732 which is an assembly of the TIMING + TEST board 1.861.063/064/065 in the box (assembly 4). The configuration may be checked by dividing the frequency written on a label on the crystal cases by 576. The system controller compares this configuration in all external sync modes (digital input included) and outputs an error message if the crystal frequency does not confirm to the frequency selected from a source via digital input (control word, byte 0), or when the internally set sampling frequency has no simple integer ratio to a video clock frequency.

ORIGIN	LINES	FRAMES	RELATIONSHIP TO SAMPL. FREQUENCIES			
		sec.	32	44.1/1.001	44.1	48
NTSC monochrome	525	30	(15/16)	---	1470	1600
NTSC color	525	30/1.001	---	1470	---	(8008/5)
PAL monochr./col.	625	25	1280	---	1764	1920
FILM	---	24	---	---	---	2000

In all cases where no simple integer ratio exists (denoted by --- or numbers in brackets) an error message is displayed in the LC-display, reading "no integer ratio", and the red pilot-LED "error" on top of the secondary keyboard is flashing.
The sampling frequency can be selected from three different sources: by an external sync source (e.g. digital input), by the reference time (RT) track or from any keyboard. The system controller reacts to the three sources in the above mentioned hierarchical order (exception: DIGITAL input and PLAY mode). It means (as an example) that a tape may be reproduced at the wrong speed, when the digital input dictates a different sampling frequency then the one indicated on the reference time track.
Selecting the sampling frequency is possible from ANALOG or DIGITAL input mode, but only when bits 6 and 7 of byte 0 of the channel status data of the digital source are set to 00. The receiving recorder selects default 48 kHz (when the crystal configuration is accordingly) and enables manual override or auto set.
Default: SAMPLING RATE HIGH.

SYNCHRONIZER ON/OFF (No. 023) KEYS/MODE

KEY SYNCHRONIZER OFF

Signal /SR-VRSPD/ of the synchronizer/parallel remote connectors is not considered. Sync of the recorder is derived either from an internal or external source as selected. When a synchronizer is connected to the recorder in this mode, the function ASCII RS-232 MODE (in the deck alignment menu) should be set to NO ECHO (no terminal mode) because the synchronizer requests status information and not commands from the transmitting source.

KEY SYNCHRONIZER ON

When the recorder is set to react to an external source it is by definition in slave mode; that means it expects external sync!

Chase Phase

The recorder reacts to the levels of the signal /SR-VRSPD/ of the synchronizer parallel remote connector. ASCII RS-232 mode is automatically set to NO ECHO, varispeed disabled. When this signal is logical zero, the recorder is said to be in 'chase phase', meaning that its tape speed is controlled by the synchronizer. In this phase, the synchronizer attempts to achieve time code coincidence between master and slave(s). The earliest instant for entry in the next phase is indicated by the signal /RANGEOK/ from the recorder to the synchronizer (see instruction set, command MS?, par. 2.10.5). When signal /SR-VRSPD/ is low the processors initiate the equivalent hardware commands

1	INPUT ANALOG
2	SYNC IN SYNCHRONIZER
3	SYNC IN EXTERNAL

in this sequential order.

Due to possible instabilities there is no Reference Time readout as long as SYNC IN SYNCHRONIZER is selected. The last valid RT Control Word is frozen, meaning that sampling frequency, format version and auxiliary track format information is not updated during the chase phase.

Phaselock Phase

When the signal /SR-VRSPD/ is logical one, the recorder is said to be in 'phaselock phase', meaning that its internal timing can be locked to an external source (no external reference may be required in master mode). For this, the recorder requires correct preadjustment. Two general cases of user set-up's are checked by the master processor: the case DIGITAL input active and valid: user set-up = INPUT DIGITAL. The processors initiate the equivalent hardware commands

1	SYNC IN DIG INPT
2	SYNC IN EXTERNAL
3	INPUT DIGITAL

in this sequential order.

Or the case DIGITAL input not active or non-valid: the master processor checks the input setting. In case of INPUT ANALOG it checks SYNC IN INT/EXT. If SYNC IN INT is set, the processors transmit the equivalent hardware commands to initialize stand-alone operation with analog input:

1	INPUT ANALOG
2	SYNC IN INTERNAL

In case of SYNC IN EXT, the master procesor checks the synchronizing source and the SYNC IN BAL/UNBAL setting and the processors send the equivalent hardware commands:

1	INPUT ANALOG	
2	SYNC IN BAL	(or)
2	SYNC IN UNBAL	
3	SYNC IN WORD CLK	(or)
3	SYNC IN DIG INPT	(or)
3	SYNC IN VID EBU	(or)
3	SYNC IN NTSC B/W	(or)
3	SYNC IN NTSC COL	(or)
4	SYNC IN EXTERNAL	

If the setting contains SYNC IN SYNCHR, a remaining error message "illegal sync source" is displayed as long as the condition SYNC IN EXT and SYNC IN SYNCHR is established (valid for SYNCHRONIZER ON condition only). The recorder transmits the command /TTLOCK/ as soon as phaselock is achieved via serial remote control port (see instruction set, command MS?, par. 2.10.5). All other commands from the keyboard remain active in both phases.
According to the mute setting of the synchronizer interface board, the synchronization operation is audible from its earliest instant (valid data from tape) to the locking process to any source, except when set to lock to digital input.
The capture time of the VCXO-PLL is in the range 300 ... 1100 msec, depending on synchronizing source. During this periode, the outputs are muted and the recorder is free- running regarding time code and regarding phase lock.
ON/OFF key. Default: SYNCHRONIZER ON.

CH CONTR: PAR/INDIV (No. 025) KEYS/MODE

The channels can either be operated in parallel or individually from either of the two columns of the Channel Control panel (CH1, CH2).
ON/OFF key. Default: CH CONTROL: INDIVIDUAL.

CHANNEL 1: SAFE/READY (No. 030) KEYS/MODE

CHANNEL 2: SAFE/READY (No. 033) KEYS/MODE

In SAFE mode, the tape is protected from overwriting. In READY mode, the recorder is ready for recording (pressing the key RECORD is necessary). Single channels can be set into SAFE status from RECORD mode (RECORD quit) if the key CHANNEL CONTROL: PARALLEL/INDIVIDUAL has been set to INDIVIDUAL. To enter RECORD mode again: activate READY key and press RECORD additionally. IN REPRODUCE mode, both SAFE and READY keys are enabled.
See also par. 2.5.7: Record.
MASTERSAFE activated overrides the READY function.
Default: SAFE.

TIME CODE: SAFE/READY (No. 036) KEYS/MODE

In SAFE mode, the time code track is protected from overwriting. In other respects refer to the SAFE/READY functions of the main channels as described above.
Default: SAFE.

RT SYNC: ON/OFF (No. 039) KEYS/MODE

The RT SYNC mode is described in par. 2.5.8.
ON/OFF key. Default: OFF.

AUX 3: SAFE/READY (No. 042) KEYS/MODE

The function is similar to the SAFE/READY keys of the main channels as described above. Auxiliary 3 track must be available to carry different information than auxiliary track 4 (dedicated for cue information) by assigning AUX 3 to DATA (key 44 below).
Default: SAFE.

MASTER SAFE: ON/OFF (No. 043) KEYS/MODE

Recording inhibition (the record head is actually disconnected from any power supply source in order to improve reliability). The MASTERSAFE key is a higher ranking protection key than the SAFE switches.
ON/OFF key. Default: OFF.

ASSIGN AUX3: DATA/CUE (No. 044) KEYS/MODE

Assigns the auxiliary 3 track to record external data in DATA mode or cue right information in CUE mode. In DATA mode, the "aux" column on the Channel Control panel is active and the LED "aux4mix" (pilot lamp of the status display field) indicates that auxiliary track 4 carries a mix (sum) of both main channels.
IMPORTANT: the configuration of the auxiliary tracks is recorded on the reference time track. In principle, it is therefore not possible to change the function, after reference time has been written! This may be a problem when a recording has been made with both cue channels carrying cueing information and when thereafter one cue channel should be accessible for additional data (e.g. PQ-channel data for CD-mastering). It is therefore possible to overwrite the auxiliary 3 track only when key 45 below is set to MANUAL position. Otherwise, the tape has to be copied with a second recorder appropriately set-up.
Default: CUE.

AUX3+AUX4:MANUAL/AUTO (No. 045) KEYS/MODE

The recorder follows the information contained in the reference time (RT) track (control word) when in AUTO mode. In MANUAL mode it is possible to overwrite auxiliary track 3, although the flag in RT is set to stereo cue mode. Refer to the description of key 44 above for an example where this could be necessary. When MANUAL is selected, an error message "auto mode disabled" may appear as long as the setting of key 44 does not correspond to the auxiliary track format flag written on the reference time track (note that reference time is overwritten in stereo record mode only!).
Default: AUTO.

CUE: UNMODULATED/AUTO (No. 046) KEYS/MODE

The key enables playback of tapes on which the cue track(s) have originally been written in modulated form. The flag on the reference time (RT) track (see par. 2.5.19) is then set for modulated. If this tape is now overwritten using a conventional bias or direct recording method, the flag on the RT track is no longer valid. When this tape should be

reproduced on a D820X again, its playback electronics have to be set to UNMODULATED.
It is necessary to select UNMODULATED only, when the flag on the reference time track does not correspond with the actual recording method used for the cue tracks. When set back to AUTO allow for some time to switch back to the mode indicated on the reference track (playback of a tape is necessary!). Default playback after UNMODULATED setting: unmodulated.
When UNMODULATED is selected, an error message "auto mode disabled" may appear as long as the setting of key 46 does not correspond to the auxiliary track format flag written on the reference time track (note that reference time is overwritten in stereo record mode only!).
Default: AUTO.

CUE: MODULATED/AUTO (No. 047) KEYS/MODE

The key enables playback of tapes with cue track(s) originally written with a conventional bias or direct recording method, but overwritten in modulated form. Due to this, the wrong condition is written on the reference time track and this is automatically selected when in AUTO mode. It can be forced to play modulated recordings when set to position MODULATED. When set back to AUTO allow for some time to switch back to the mode indicated on the reference track (playback of a tape is necessary!). Default playback after MODULATED setting: modulated.
When MODULATED is selected, an error message "auto mode disabled" may appear as long as the setting of key 47 does not correspond to the auxiliary track format flag written on the reference time track (note that reference time is overwritten in stereo record mode only!).
Default: AUTO.

HIGH PASS FIL: ON/OFF (No. 048) KEYS/MODE

This digital filter removes DC offset of the analog-to-digital converter when activated. The cutoff frequency (-3 dB point) is 0.5 Hz. It exhibits single pole rolloff characteristics and introduces no phase distortion and no ripple.
Due to varying levels of quantizing noise (finite word length effects) the clipping LED's may flicker when the filter is inserted and when a full scale signal is applied to the input.
ON/OFF key. Default: OFF.

QUALITY DISP: ON/OFF (No. 049) KEYS/MODE

Enables/disables the local signal quality display indication of the tape deck and on the display panel. See par. 2.5.22 (Display Panel) for more information on the signal quality display.
ON/OFF key. Default: ON.

LEVEL DISP: NORM/INPT (No. 050) KEYS/MODE

Indication mode for the bargraph level display located in the Display panel. In NORMAL mode, the indication is according to the keys INPUT and REPRO of the Channel Control panel (CCP).
In INPUT mode, the display reacts similar to the AUTOINPUT A mode. It shows input levels in STOP, EDIT and WIND modes. The feature may be helpful when the display panel is installed in a remote location (e.g. in a mixing console).
Default: NORMAL.

SYNC IN: EXT/INT (No. 051) KEYS/MODE

In internal (INT) mode, the D820X generates its own sync (timing) signals. The only possible configuration for this is with ANALOG INPUT and INT SYNC.
When the recorder is set to react to an external source (EXT) it is by definition in slave mode; that means it expects **external** sync!
Several external sync sources may be selected as listed below.
Default: INTERNAL.

SYNC IN: BAL/UNBAL (No. 052) KEYS/MODE

In BALANCED mode, inputs from the DSUB25 connector labeled "external clock" are accepted in RS-422 electrical interface standard. In UNBALANCED mode, the signals are routed from the BNC connectors "videoclock" input or "wordclock" input. When composite video is fed to the videoclock input, UNBALANCED mode has to be selected, together with the corresponding video standard. When time code is recorded additionally, select the appropriate frame rate for coincident output of the main (digitalaudio) channels and time code.
Default: UNBALANCED.

SYNC IN: WORD CLK Y/N (No. 053) KEYS/MODE

It can be either balanced (from DSUB25 connector labelled "external clock") or unbalanced wordclock (from the BNC connector). The crystal configuration of the recorder must correspond to the external frequency. The board Timing + Test 1.861.063/064/065 carries jumper connectors to select either 75 ohm or high impedance line termination.
ON/OFF key. Default: ON.

SYNC IN: DIG INPT Y/N (No. 054) KEYS/MODE

Digital input according to the professional AES/EBU standard or, according to the consumer format (data or sync only) is selected (XLR-connector labeled "DI" on the box). The recorder is in slave mode. It is configured (sampling frequency, emphasis, etc) according to the control word of the master device. See key 18, INPUT DIGITAL for more information.
ON/OFF key. Default: OFF.

SYNC IN: VID EBU Y/N (No. 055) KEYS/MODE

Either balanced videoclock (from the DSUB25 connector labeled "external clock") or composite video (from the BNC connector) with 25 frames per second. The crystal configuration of the recorder must correspond to the external frequency (see table under key 20, SAMPLING RATE). If time code is recorded additionally, select the appropriate frame rate for coincident output of digitalaudio and time code. See table below key 057 for relationships between video and digital audio sampling frequencies.
ON/OFF key. Default: OFF.

SYNC IN NTSC B/W: Y/N (No. 056) KEYS/MODE

Either balanced videoclock (from the DSUB25 connector labeled "external clock") or composite video (from the BNC connector) with 30 frames per second. The crystal

configuration of the recorder must correspond to the external frequency (see table under key 20, SAMPLING RATE). If time code is recorded additionally, select the appropriate frame rate for coincident output of digitalaudio and time code. See table below key 057 for relationships between video and digital audio sampling frequencies.
ON/OFF key. Default: OFF.

SYNC IN NTSC COL: Y/N (No. 057) KEYS/MODE

Either balanced videoclock (from the DSUB25 connector labeled "external clock") or composite video (from the BNC connector) with 29.97 frames per second. The crystal configuration of the recorder must correspond to the external frequency (see table under key 20, SAMPLING RATE). If time code is recorded additionally, select the appropriate frame rate for coincident output of digitalaudio and time code.

Video-/Film-Clocks VS. Sampling Frequencies

ORIGIN	LINES	FRAMES	RELATIONSHIP TO SAMPL. FREQUENCIES			
		sec.	32	44.1/1.001	44.1	48
NTSC monochrome	525	30	(15/16)	---	1470	1600
NTSC color	525	30/1.001	---	1470	---	(8008/5)
PAL monochr./col.	625	25	1280	---	1764	1920
FILM	---	24	---	---	---	2000

ON/OFF key. Default: OFF.

SYNC IN SYNCHR: Y/N (No. 058) KEYS/MODE

The signal /SR-VRSPD/ of the synchronizer parallel remote connector controls the recorder. Plus/minus 30 % frequency deviation from the nominal frequencies (see 1.7, interfacing specifications) is allowed.
Due to possible instabilities there is no Reference Time readout as long as SYNC IN SYNCHRONIZER is selected. The last valid RT Control Word is frozen, meaning that sampling frequency, format version and auxiliary track format information is not updated during the chase phase.
ON/OFF key. Default: OFF.

SYNCOUT SECT CLK: Y/N (No. 059) KEYS/MODE

SYNCOUT WORD CLK: Y/N (No. 060) KEYS/MODE

Either word- or sectorclock is selected to appear at the appropriately labeled BNC connector and at the DSUB25 connector "external clock". Par. 1.7 (interfacing specifications) gives more details about it. The board Timing + Test 1.861.063/064/065 carries a jumper connector to select either RS-423 or pseudo-TTL electrical interfacing.
ON/OFF key. Default: WORD CLOCK.

IGNORE DI C WORD: Y/N (No. 064) KEYS/MODE

When set to ON, the recorder ignores the information contained in the control word of the professional or consumer digital input standard according to the AES/EBU or to the manufacturers of consumer equipment. If the recorder receives a control word not corresponding to professional audio requirements, and error message "ILLEGAL DI FORMAT" is displayed.

ON/OFF key. Default: OFF.

MASTERING ON: Y/N (No. 070) KEYS/MODE

Digital input 2 (DI2) active in MASTERING ON mode. A signal fed to DI2 is routed to the Analog Output board. Timing signals for the Analog Output board are not derived from DI2, however. This indicates that DI2 is no external sync input. All timing signals for the Analog Output board are derived from the internal master timing of the recorder in order to obtain best performance regarding signal-to-noise ratio and nonlinear distortion. The main purpose of this function is to disconnect the Analog Output from the decoding electronics. An external processing device with digital in- and outputs according to the profesional AES/EBU format can the be connected between DO and DI2 (insert). This external device could be a delay unit, retarding the main channels fed to a cutting lathe. Applications for the MASTERING ON function are therefore primarily seen in the analog disk mastering field.
ON/OFF key. Default: OFF.

TEST: ON/OFF (No. 070) KEYS/MODE

Press STORE and a list of electronics-to-electronics loops appears which can be selected with the cue wheel (see below). Try both directions if the LC display does not change in one direction.

0: no test - through	(ee-loop 0)
1: before write head	(ee-loop 1)
2: x-form to dasy	(ee-loop 2)
3: codec to codec	(ee-loop 3)
4: dapro to dapro	(ee-loop 4)
5: adc to dac	(ee-loop 5)
6: left bef write h	(ee-loop 1, left channel only)
7: right bef write h	(ee-loop 1, right channel only)
8: stop rf track	(task for reference time track stopped)

Loop 0: normal operation, no loop connected.

Loop 1: Service loop only. It connects immediately before the head drivers located on the Write Amplifier with the comparators on the Detector board. This loop preserves the delay structure of the recorder (the head delay of 152 blocks is not included). Single channel operation is possible with caution (see D820X manual Vol. III, sect. 3, par. 1.1) via ASCII serial interface only. This loop permits testing of all PCM electronics, except write head drivers, head amplifier, playback amplifier and the lowpass filter and comparator sections on the Detector board. The 8 LED on the Transformatter board are not illuminated in this loop. Disconnect the Adaptive Run Processor board to confirm that the loop has been properly established (not under power!). The signal quality display should remain stable with no correction indicated and the 7 LED's on the Adaptive Run Processor should not be flickering (refer to par. 2.5.6).

Loop 2: this loop connects the modulator to the demodulator in the Transformatter board. It is established from the ASCII serial interface with command SRH. It preserves the delay structure of the recorder. Stereo operation only.
Watch the 8 LED which indicate CRC errors. They should not be illuminated in this loop. The signal quality display should remain stable with no correction indicated.

Loop 3: it connects the output of Codec with its input at the Transformatter interface. The 8 LED on the Transformatter board are illuminated because no valid information

reaches this board. The signal quality display should remain stable with no correction indicated.

Loop 4: this is the INPUT and local REHEARSE loop. It connects the Data Processor (DAPRO) output to the data procesor input, in front of Codec. The digital output gains are not included in this loop.
The signal quality display is not active and the 8 LED on the Transformatter are illuminated.

Loop 5: it is located at the input of the Data Procesor (DAPRO) and connects the output of the analog-to-digital converter with the input of the digital-to-analog converter, with only several shift registers of the Data Processor (DAPRO IF board) in between. The loop permits to check the analog performance only. The signal quality display is not active and the 8 LED on the Transformatter are illuminated.

Stop reference track: it is used during adjustment of the write currents. It stops the entire reference time task. Type "TASK" on the keyboard of a terminal or personal computer connected to the "Test" connector and the state of all implemented tasks is listed.

To exit from TEST mode, press NEXT. The pilot LED "test" flashes as long as one of the functions is active (except loop 0).
On/OFF key. Default: OFF.

REHEARSE (No. 101) KEYS ONLY

Allows simulation of punch-in operation. Preparation key; active in RECORD mode only. The PLAY key flashes in reproduce mode. When RECORD and PLAY are selected, record mode is simulated for the digitalaudio tracks. However, recording mode is not started. Pressing PLAY restores reproduction mode. Selecting the function: from spooling, PLAY, STOP, EDIT, SHUTTLE, SHUTTLE stored, LOC and ROLLBACK; conditions for REHEARSE: the corresponding channel must be switched to READY. Canceling the function: by pressing REHEARSE again.
Local REHEARSE (from keyboard) establishes the INPUT loop (EE 4), single channel operation is possible.
REHEARSE from the ASCII serial interface port (commands SRH and CRH) connects loop 2. It preserves the delay and blocking structure of the recorder. Stereo operation only. Watch the yellow pilot lamp on top of the secondary keyboard for proper activation of the function.
Note that there is no REHEARSE mode for time code or auxiliary track 3. It appears more convenient to edit auxiliary data in solid state memories than on tape.
ON/OFF key. Default: OFF.

TAPE GUARD A: RED/NO (No. 201) KEYS/MODE

Reduction of the spooling speed shortly before the tape is unthreaded (tape out). From the speed difference between the two reels the recorder can detect that the corresponding supply reel contains relatively few layers of tape.

TAPE GUARD B: STOP/NO (No. 202) KEYS/MODE

The transport stops fast winding shortly before the tape is unthreaded (tape out). From the speed difference between the two reels the recorder can detect that the corresponding supply reel contains relatively few layers of tape.

VARISPEED %: Y/N (No. 210) KEYS/MODE

VARISPEED HT: Y/N (No. 211) KEYS/MODE

VARISPEED IPS: Y/N (No. 212) KEYS/MODE

VARISPEED: %/IPS/HT (No. 213) KEYS/MODE

Keys for defining the VARISPEED display format. Indication of the deviation in percent of the nominal speed, in semitones, or inches per second. Either an individual key (functions 210...212) or a "ring key" (advances one step whenever the key is pressed, function 213) can be programmed for each format.

VS INDIC.ENHANCED (No. 214) KEYS/MODE

If activated flashing of the spooling keys ◄ and ► can be selected with this ON/OFF function in VARISPEED mode.

FADER START A (No. 220) KEYS/MODE

FADER START B (No. 221) KEYS/MODE

FADER START C (No. 222) KEYS/MODE

FADER START D (No. 223) KEYS/MODE

With the fader start circuit it is possible to start the recorder remotely into reproduce mode. FADER START mode can be prepared (FADER START READY) with a switch that interconnects pin 6 (signal SR-FADRY) with pin 1 (ground) of the parallel control socket. An AC or DC voltage from 5 V to 24 V can be applied to pins 11 and 12; the recorder is started in playback mode. Preparation is also possible with the programmable FADER key on the local keyboard or with the serial remote control, or with the FADER key on the parallel remote control.

Four programmable possibilities:

FADER A:

without preparation key (FADER START READY)

FADER B:

FADER START with enable key (FADER START READY), local keyboard also active when FADER START enabled. The local keyboard will be disabled after FADER START; default programming.

FADER C:

Same as FADER START B, except local keyboard disabled when FADER START enabled.

FADER D:

FADER START with enable key (FADER START READY), local keyboard also active when FADER START enabled. After the FADER START, the built-in monitor speaker (not the headphones) is muted. If one of the local keys is operated in PLAY mode after the FADER START operation has been performed, muting of the monitor speaker is canceled. If FADER START is not enabled, actuation of the FADER switch does not change the operating mode of the recorder.
Detailed description of the FADER START functions: see par. 2.5.15.
Default: FADER START B.

REWIND (◄) (No. 301) KEYS/MODE

Rewind with maximum (programmed) spooling speed. Selecting the function: from FORWARD, STOP, PLAY/REC, SHUTTLE stored, all LOC functions, and CUE. Canceling the function: by pressing FORWARD, STOP, PLAY, SHUTTLE, SHUTTLE BAR, all LOC functions; in synchronizer mode by pressing LOCK. The spooling speed can be defined in the alignment deck block.
Default parameter: 10 m/s.

FORWARD (►) (No. 302) KEYS ONLY

Fast forward with maximum (programmed) spooling speed.
Selecting/canceling conditions: same as REWIND.

LIBRARY WIND (No. 303) KEYS ONLY

In conjunction with FORWARD or REWIND, preselection of this function causes spooling with reduced, defined speed (preselectable from 0.1 to 15 m/s, in steps of 0.1 m/s). Canceling the function: by pressing LIBRARY WIND again. The reduced spooling speed can be defined in the alignment deck block.
Default parameter: 2.5 m/s.

PLAY (No. 304) KEYS ONLY

Playback with the selected tape speed. Canceling the function: by FORWARD, REWIND, STOP, SHUTTLE, SHUTTLE BAR, all LOC functions.

STOP (No. 306) KEYS ONLY

All tape transport functions are canceled by this key.

RECORD A (No. 307) KEYS ONLY

Record mode, only possible in conjunction with PLAY. Selection of the function: by simultaneously pressing RECORD and PLAY. Canceling the function: see PLAY, drop-

out by pressing PLAY also possible (recorder reenters PLAY mode without interruption). Illumination of the key is inhibited if MASTER SAFE is activated or if none of the columns on the Channel Control panel is set to READY.
The RECORD mode is described with more detail in chapter 2.5.7.

RECORD B	(No. 308) KEYS ONLY

Record mode, analogous to RECORD A, except: if the recorder is already in reproduce mode, recording can be activated by pressing the RECORD key only.

EDIT	(No. 309) KEYS ONLY

Activation of the SET/CUE wheel. With the SET/CUE wheel the tape can be fine-positioned by means of the spooling motors. Selecting the function: from STOP, FORWARD, REWIND, PLAY. Canceling the function: with STOP, FORWARD, REWIND, PLAY, CUT, SET TIMER, SET ADDR, SET VARISPEED, SHUTTLE BAR, all LOC functions. When the tape is unthreaded in EDIT mode, the tape guide assembly remains in EDIT position. When the STOP key flashes after power-on, the tape guide assembly can be moved into EDIT position by pressing the EDIT key. The EDIT position is reached by pressing EDIT regardless of whether the tape is threaded or not.

CUT	(No. 310) KEYS ONLY

Automatic positioning of the tape address located at the CUE point (reproduce head gap) to the position of the scissors. Selecting the function: from STOP (in reproduce mode only). Canceling the function: by pressing STOP, PLAY, or by cutting the tape (tape out).

TRANSFER	(No. 311) KEYS ONLY

Multifunction key. Buffering of the current tape counter address. The buffered tape address is transferred into the corresponding LOC memory by pressing one of the keys LOC 1...5. Selecting the function: possible at any time. Canceling the function: by storing in LOC memory or by pressing TRANSFER again.

HOLD	(No. 312) KEYS ONLY

Key for "freezing" the current tape counter reading in any condition (functions also when the tape counter is in stopwatch mode). The frozen counter reading can be transferred into one of the LOC memories: either by pressing one of the keys LOC1...5, in which case the counter continues to advance and the tape is positioned at the stored address by pressing the same LOC key again; or by pressing TRANS and subsequently one of the keys LOC1...5, in which case the counter reading remains "frozen". Pressing the same LOC key again reenables the tape counter, and the LOC process is only started when the LOC key is pressed a third time.

LOCATOR 1	(No. 313) KEYS ONLY
LOCATOR 2	(No. 314) KEYS ONLY
LOCATOR 3	(No. 315) KEYS ONLY
LOCATOR 4	(No. 316) KEYS ONLY
LOCATOR 5	(No. 317) KEYS ONLY

Automatic searching of the stored address in spooling mode; preselection of PLAY or PLAY and RECORD is possible (keys of the preselected function flash for as long as the LOC process is not yet terminated). Indication of target address: in STOP status by simultaneously pressing STOP and the corresponding LOC key; during a LOC operation: by continuously pressing the corresponding LOC key. All LOC addresses remain stored even after power-down. Selecting the function: from PLAY/REC, REWIND, FORWARD, LOC, SHUTTLE, EDIT. Canceling the function: with STOP, LOC, REWIND, FORWARD, SHUTTLE, SHUTTLE BAR.
More on locators can be found in chapter 2.5.12.

ZERO LOCATOR	(No. 318) KEYS ONLY

Automatic searching of the tape address 0.00.00.0 in spooling mode; preselection of PLAY or PLAY and RECORD possible. Selecting/canceling the function: see LOC1...LOC5.

LOC START STOP	(No. 319) KEYS ONLY
LOC START PLAY	(No. 320) KEYS ONLY
LOC START REC	(No. 321) KEYS ONLY

Analogous to LOC1...LOC5; the LOC START address is stored automatically for each PLAY or PLAY and RECORD command. PLAY or STOP or RECORD is automatically initiated when the target address is reached. Selecting/canceling the function: see LOC1...LOC5.

ROLLBACK STOP	(No. 322) KEYS ONLY

ROLLBACK PLAY	(No. 323) KEYS ONLY

ROLLBACK REC	(No. 324) KEYS ONLY

The recorder spools automatically backward by a preselected time. ROLLBACK always relates to the current tape counter reading (also in other indication modes). PLAY or STOP or RECORD is automatically initiated after the target address has been reached. Selecting the function: from STOP, PLAY, RECORD, EDIT. Canceling the function: by pressing STOP, REWIND, FORWARD, PLAY, PLAY and RECORD, SHUTTLE, SHUTTLE BAR, all LOC functions. The ROLLBACK time can be defined in the alignment deck block.
Default value: 15 seconds.

TAPE DUMP A	(No. 327) KEYS ONLY

TAPE DUMP B	(No. 328) KEYS ONLY

Dump edit mode, take-up motor stopped. The tape counter is active and supplied with information from the tacho of the capstan motor (TAPE DUMP A), or the tape counter is blocked (TAPE DUMP B). Selecting the function: only possible from STOP mode. Canceling the function: by pressing TAPE DUMP a second time or with STOP.

TAPE DUMP C	(No. 329) KEYS ONLY

TAPE DUMP D	(No. 330) KEYS ONLY

Tape dump mode with preparation, the take-up motor is stopped. The tape counter is active and supplied with information from the tacho of the capstan motor (TAPE DUMP C), or the tape counter is blocked (TAPE DUMP D). Selecting the function: only possible from STOP mode. Preparation by means of TAPE DUMP, start of tape dump mode with PLAY, interruption with STOP. Canceling the function: by pressing TAPE DUMP a second time (only possible in STOP mode).
Default: TAPE DUMP A.

LIFTER A	(No. 332) KEYS ONLY

LIFTER B	(No. 333) KEYS ONLY

When activated during spooling, it causes resetting of the tape lift pin and engagement of the tape guide assembly so that the tape is pressed against the reproduce head. The cue tracks become audible, if the tape speed is within a certain range and the AUTOMUTE function is not active (affects the line outputs only, not the internal speaker) for as long as the tape is in contact with the head. Some synchronizers may require this function to read time code in fast forward or rewind.

LIFTER A: momentary push button, LIFTER B: ON/OFF key.

Selecting the function: during REWIND, FORWARD, LOC and ROLLBACK functions. Canceling the function: by releasing the LIFTER key (LIFTER A) or by pressing the LIFTER key a second time (LIFTER B).

START/STOP (No. 334) KEYS ONLY

Used in conjunction with WATCH for relative time measurements, or to START and STOP accumulating tape errors in "show quality" mode from terminal or personal computer only (see D820X manual, Vol. III, sect. 2) to assess the performance of the digitalaudio electronics or of the tape. The key located in the Display panel is used also to enable CAL GAINS, UNCAL GAINS, HEADROOM and PEAK mode, when pressed simultaneously with the desired key.

RESET TIMER (No. 335) KEYS ONLY

Key for resetting the tape counter display, the LAP/WATCH display, the reference time display and (in "show quality" mode) the error counters. Only the counter reading shown on the display will be set to zero. The corresponding counter reading remains at zero until the key is released.

SET TIMER (WATCH) (No. 336) KEYS ONLY

When this key is pressed the momentary content of the tape counter is transferred into a buffer. With the CURSOR keys the display position (h, min, s, 1/10 s) is selected which can subsequently be increased or decreased continually by turning the SET/CUE wheel clockwise or counterclockwise respectively. When STORE is pressed the changed counter reading is transferred to the tape counter. Canceling the function: by pressing SET TIMER a second time or with SET ADDR, SET VARISP.

SET ADDRESS (No. 337) KEYS ONLY

Pressing this key changes the tape counter display over to 0.00.00.0. With the CURSOR keys the display position (h, min, s, 1/10 s) can be selected which can subsequently be continually increased or decreased by turning the SET/CUE wheel clockwise or counterclockwise respectively. The set address is stored in a LOC register by pressing TRANSFER and one of the LOC keys. The content of the tape counter reappears when the store function has been completed. Canceling the function (only if store function has not been performed): by pressing SET ADDRESS a second time, a LOC or ROLLBACK function, SET TIMER, SET VARISPEED.

SET VARISPEED (No. 338) KEYS ONLY

Input of varispeed. Switches the service display over to VARISPEED indication. The deviation from the nominal speed is indicated in the desired format. The indicated value can be varied with the SET/CUE wheel. The format is entered with one of the VARISPEED DISPLAY functions 210...213. SET VARISPEED is not possible during audio alignment (SET/CUE wheel is needed for alignment). Canceling the function: by pressing SET VARISPEED a second time, or by pressing SET TIMER.

VARISPEED ON/OFF (No. 339) KEYS ONLY

Activates the variable tape speed; the selected value is indicated on the service display. The red "varispeed" pilot lamp flashes as soon as the VARISPEED function is active. If SET VARISPEED is also selected, the tape speed can also be varied during playback by means of the SET/CUE wheel. If EDIT is also selected it is no longer possible to vary the speed with the SET/CUE wheel because the function of the SET/CUE wheel is required for the EDIT function. Canceling the function: by pressing VARISPEED ON/OFF a second time.

REMOTE A (No. 345) KEYS ONLY

Activates the parallel and/or serial remote control; the local keyboard is disabled. Selecting the function: only from STOP mode.
See par. 2.5.14.

REMOTE B (No. 346) KEYS ONLY

Activates the parallel and/or serial remote control. The local keyboard remains enabled. Selecting the function: only from STOP mode.
See par. 2.5.14.

SHUTTLE BAR (No. 347) KEYS ONLY

Key for storing a SHUTTLE speed that has been selected with the SHUTTLE wheel. Selecting the function: while actuating the SHUTTLE wheel. Canceling the function: with all tape transport
commands, LOC and ROLLBACK functions.
See par. 2.5.9: Spooling, Shuttle.

TIME display (No. 355) KEYS ONLY

Normally a ring key. Displays absolute and relative tape counters (tacho roller pulses) plus time code plus reference time. This sequential order is obtained and assigned to TIME when function 360 is selected. The relative counter display is indicated with a prefix "l", the time code with "t" and the reference time with "r". The display format can be selected in the alignment deck menu (stop and move format, leading zeroes) and resetting of all functions except time code is performed with the RESET TIMER key. The function is duplicated in the Display panel (WATCH function separately). In absolute time mode, LOC ZERO relates to the zero position of the absolute counter.
Par. 2.5.13 contains additional information on TIME.
Canceling the function: by pressing WATCH display.
Default: function 360.

WATCH display (No. 356) KEYS ONLY

Changeover of tape display to a second counter which (like the normal tape counter) is supplied with pulses from the tacho roller. When LAP/WATCH is active, an "l" is shown in the first position of the tape counter display. The counter is reset to zero with RESET TIMER. In LAP/WATCH mode, LOC ZERO relates to the zero position of the LAP/WATCH counter.

WATCH display is automatically chosen in "show quality" mode from an externally connected terminal or personal computer. Do not leave WATCH mode as long as tape errors should be accumulated.
Canceling the function: by pressing TIME display.

RT display (No. 357) KEYS ONLY

Displays sector addresses of the reference time track. Resetting is performed with the RESET TIMER key. Setting to a specific address is not possible. The display format can be selected in the alignment menu. Refer to par. 2.5.19 for more information on reference time. Canceling of the function: press any other TIME key.

TIMECODE DISPLAY (No. 358) KEYS ONLY

Displays time code of an external generator connected to the time code input. Resetting is performed at the external generator only. Refer to par. 2.5.18 for more information on time code. Canceling of the function: press any other TIME key.

TIME/WATCH DISPLAY (No. 359) KEYS ONLY

Ring key for display of absolute time or relative time.

TIME/WATCH/RT/TC DIS (No. 360) KEYS ONLY

Ring key for display of all supported time modes of the D820X. Canceling with any other time function.
Default programming of the TIME key.

UNLOAD (No. 361) KEYS ONLY

See par. 2.5.5.

NO FUNCTION (No. 362) KEYS ONLY

It is used to desactivate certain keys in order to prevent erroneous operation.

25 F/SEC Y/N (No. 401) KEYS/MODE

29.97 F/SEC Y/N (No. 402) KEYS/MODE

30 F/SEC Y/N (No. 403) KEYS/MODE

25/29.97/30 F/SEC (No. 404) KEYS/MODE

25/29.97 F/SEC (No. 405) KEYS/MODE

29.97/30 F/SEC (No. 406) KEYS/MODE

Sets the delay time in time code reproduction according to the frame rate. It is necessary that the frame rate settings of an external generator or of a tape matches that of the recorder in order to align time code correctly with digitalaudio at the output of the recorder. The alignment on tape is always warranted.
The time code display and the corresponding function of the serial interface port (TCD) is interpolated when time code readout from tape is interrupted (i.e. during dropouts or in WIND mode). Interpolation is indicated by a point which appears after the prefix "t". The TC line output (XLR connector) is never interpolated.
If a time code which is written on tape does not correspond to the indicated frame rate, the interpolation mathematics will be wrong. This is visible when a 25 Hz time code is reproduced with a 30 or 29.97 Hz setting. The error-point is then flashing periodically. The other way around (reproducing a 29.97 or 30 Hz code with a 25 Hz setting) can not be recognized easily. The displayed code is not valid when settings do not match.

DISPLAY CODE: Y/N (No. 407) KEYS/MODE

The LED displays in the transport or in the Display panel show actual time code time as written on tape or fed to the recorder from an external generator.

DISP. USER BITS Y/N (No. 408) KEYS/MODE

The LED displays are set to show the user bits contained in the time code frames.

DISP UNASS. BITS Y/N (No. 409) KEYS/MODE

The LED displays are set to show unassigned bits (dropframe, etc.) contained in the time code frames.

DISPLAY USER/CODE (No. 410) KEYS/MODE

CODE/USER/UNASSIGNED (No. 411) KEYS/MODE

Ring keys for the functions described above. See par. 2.5.18 for display format.

TC: UNMODULATED/AUTO (No. 415) KEYS/MODE

The key enables playback of tapes on which the time code track has originally been written in modulated form. The flag on the reference time (RT) track (see par. 2.5.19) is then set for modulated. If this tape is now overwritten using a conventional bias or direct recording method, the flag on the RT track is no longer valid. When this tape should be reproduced on a D820X again, the playback electronics should be forced to UNMODULATED.
It is necessary to select UNMODULATED only when the flag on reference time does not correspond to the actual recording method used for the time code track. When set back to AUTO allow for some time to switch back to the mode indicated on the reference track (playback of a tape is necessary!). Default playback after UNMODULATED setting: unmodulated.
When UNMODULATED is selected, an error message "auto mode disabled" may appear as long as the setting of key 415 does not correspond to the auxiliary track format flag written on the reference time track (note that reference time is overwritten in stereo record mode only!).
Default: AUTO.

TC: MODULATED/AUTO (No. 416) KEYS/MODE

The key enables playback of tapes on which the time code track has originally been written using a conventional bias or direct recording method, but overwritten in modulated form. Due to this, the wrong condition is written on the reference time track and this is automatically selected when in AUTO mode. It can be forced to play modulated recordings when set to position MODULATED. When set back to AUTO allow for some time to switch back to the mode indicated on the reference track (playback of a tape is necessary!). Default playback after MODULATED setting: modulated.
When MODULATED is selected, an error message "auto mode disabled" may appear as long as the setting of key 416 does not correspond to the auxiliary track format flag written on the reference time track (note that reference time is overwritten in stereo record mode only!).
Default: AUTO

TC DELAY: OFF/AUTO (No. 425) KEYS/MODE

In OFF mode, it disables the time code delay which compensates the delay of the decoding electronics. The time code readout on the display panel(s) and on any remote reader (XLR connector) is then time-coincident with the signals recorded on auxiliary tracks 3 and 4 when in stereo cue mode, otherwise with auxiliary 4 only.
Overriding by remote commands is enabled in AUTO mode.
The D820X activates the time code delay in PLAY (and RECORD) mode only, when set to AUTO. The time code readout on the display panel(s) and on any remote reader is then time-coincident with the audio signal of the main (digitalaudio) channels, otherwise it is coincident with the track(s) carrying cue information.
Par. 2.5.18, Time Code Track, contains more details on time code.
Default: AUTO.

TC DELAY: ON/AUTO (No. 426) KEYS/MODE

The key activates the time code delay in ON mode, which compensates the delay of the decoding electronics. The time code readout on the display panel(s) and on any remote

reader which is connected to the serial output (XLR connector) is time- coincident with the audio signal of the main (digitalaudio) channels.
The D820X enables the time code delay in PLAY (and RECORD) mode only, when set to AUTO. The time code readout on the display panel(s) and on any remote reader is then time-coincident with the audio signal of the main (digitalaudio) channels, otherwise it is coincident with the track(s) carrying cue information.
Overriding by remote commands is enabled in AUTO mode.
Par. 2.5.18, Time Code Track, contains more details on time code.
Default: AUTO.

FUTURE USE (No. 501) KEYS ONLY

2.6.5 Programming Examples

Example 1:

Setting the hub diameter of the take-up reel to 50 mm (Cine B):

	Action	Service display indicates
	Turn programming enable switch [28] to counterclockwise stop (Allen key No. 2.5)	
	Recorder in STOP mode	LEVEL A:xx.x D: xx.x FR/SEC xx DELAY xxx
	↓/NEXT	USER SET UP ALIGMENT MODE
	↓/NEXT	ALIGNMENT AUDIO DECK AUX
	►/CURSOR	ALIGNMENT AUDIO DECK AUX
	↓/NEXT	HUB DIAMETER LEFT SET: NAB (118mm)
	↓/NEXT	HUB DIAMETER RIGHT SET: NAB (118mm)
	↓/NEXT	MAX REEL DIAMETER SET: 12.5" (318 mm)
	Set desired diameter with the SET/CUE wheel	HUB DIAMETER RIGHT SET: NAB (118mm)
	Save with STORE	
	Press 4x LAST	LEVEL A:xx.x D: xx.x FR/SEC xx DELAY xxx
	or	
	with ↓/NEXT to the next setting	SET LIBR WIND SPEED 8.0 m/s

Example 2:

Activating the AUTOMUTE function (No. 016) without a key being assigned:

	Action	Service display indicates
	Turn programming enable switch [28] to counterclockwise stop (Allen key No. 2.5)	
	Recorder in STOP mode	LEVEL A:xx.x D: xx.x FR/SEC xx DELAY xxx
	↓/NEXT	USER SET UP ALIGMENT MODE
	►/CURSOR	USER SET UP ALIGNMENT MODE
	↓/NEXT	KEY / MODE SETTING AUDIO DECK TC
	↓/NEXT	AUDIO KEYS/MODE KEYS ONLY
	↓/NEXT	F001 1/0 no key CLIP LEVEL 4dBm Y/N
	Page with SET/CUE wheel to function 016	F016 0/1 no key AUTOMUTE ON/OFF
	Change over with STORE	F016 1/0 no key AUTOMUTE ON/OFF
	Press ↑ 4x	LEVEL A:xx.x D: xx.x FR/SEC xx DELAY xxx

Example 3:

Reprogramming of the FADER START key (key no. 23, function No. 221) to AUTOINPUT B (function no. 015):

	Action	Service display indicates
	Turn programming enable switch [28] to counterclockwise stop (Allen key No. 2.5)	
	Recorder in STOP mode	LEVEL A:xx.x D: xx.x FR/SEC xx DELAY xxx
	↓/NEXT	USER SET UP ALIGMENT MODE
	►/CURSOR	USER SET UP ALIGNMENT MODE
	↓/NEXT	KEY / MODE SETTING AUDIO DECK TC
	↓/NEXT	AUDIO KEYS/MODE KEYS ONLY
	↓/NEXT	F001 1/0 no key CLIP LEVEL 4dBm Y/N
	Page with SET/CUE wheel to function 015	F015 0/1 no key AUTOINPUT B ON/OFF
	Press STORE	F015 PRESS 2nd KEY AUTOINPUT B ON/OFF
	Continue to hold down STORE, and in addition press FADER START Change over with STORE	F041 key assigned AUTOINPUT B ON/OFF F016 1/0 no key AUTOMUTE ON/OFF
	Change keytop label from FADER START to AUTOINPUT	
	Press ↑ 4x	LEVEL A:xx.x D: xx.x FR/SEC xx DELAY xxx

2.7
Degraded Operation

2.7.1
Error Messages of the Service Display

Display MASTER ERROR:
no errors detected

Cause no errors detected during selftest routine
Action none

Display MASTER ERROR:
unusual reset

Recorder functional
Cause unusual power-down, activation of reset button on Master MPU
Action press STORE
Priority 12

Display MASTER ERROR:
ram new: first used

Recorder "error" LED flashing, "error" is indicated in the secondary keyboard, recorder frozen
Cause first usage of RAM
Action press STORE, or switch mains voltage off and on
Priority 13

Display MASTER ERROR:
ram new: checksum

Recorder "error" LED flashing, "error" is indicated in the secondary keyboard, recorder frozen
Cause RAM checksum error
Action check EPROM set in Master MPU
Priority 14

Display MASTER ERROR:
key new: fatal key

Recorder "error" LED flashing, "error" is indicated in the secondary keyboard, recorder frozen
Cause key assignment of new EPROM set not identical to old set
Action press STORE; program old assignment; switch mains voltage off and on
Priority 15

Display

MASTER ERROR: ram test failed

Recorder "error" LED flashing, "error" is indicated in the secondary keyboard, recorder frozen
Cause RAM-test failed, RAM defective
Action replace RAM in Master MPU
Priority 16

Display

MASTER ERROR: version mismatch

Recorder "error" LED flashing, "error" is indicated in the secondary keyboard
Cause version mismatch between RAM and ROM
Action press STORE, continue
Priority 17

Display

MASTER ERROR: shuttle invalid

Recorder "error" LED flashing, "error" is indicated in the secondary keyboard
Cause the SHUTTLE potentiometer indicated unexpected values during start-up
Action the SHUTTLE wheel may not be deflected during start-up. Leave SHUTTLE wheel in idle position. Press STORE; switch mains voltage off and on.
Priority 18

Display

MASTER ERROR: variable corrected

Recorder no action, warning
Cause invalid variable value (parameter outside admissible range)
Action Master selects default value; press STORE, continue.
Priority 19

Display

MASTER ERROR: ram new: load failed

Recorder no action
Cause loading error during parameter backup
Action try again
Priority 20

Display

MASTER ERROR: illegal sync source

Recorder "error" LED flashing
Cause key SYNCHRONIZER ON active and function 058 SYNC IN SYNCHR selected (see key 023: SYNCHRONIZER ON/OFF)
Action desactivate one of both keys
Priority 39

Display MASTER ERROR:
> in burn-in mode! <

Recorder in special operating mode (burn-in)
Cause burn-in test
Action set jumper on Master MPU to normal position
Priority 8

Display TAPE DECK ERROR:
no errors detected

Cause no errors detected during seftest
Action none

Display TAPE DECK ERROR:
+5 V down

Recorder "error" LED might be flashing; not functional
Cause 5V supply failure
Action check indicators on right hand side below tape deck. Replace fuses if necessary; repair or replace boards or assemblies (tape deck power supply)
Priority 21

Display TAPE DECK ERROR:
power down

Recorder "error" LED might be flashing; not functional
Cause any power supply error
Action check indicators on right hand side below tape deck. Replace fuses if necessary; repair or replace boards or assemblies (tape deck power supply)
Priority 22

Display TAPE DECK ERROR:
motor supply down

Recorder "error" LED flashing; not operational
Cause motor supply voltage down
Action replace fuses, repair or change boards and/or assemblies
Priority 23

Display TAPE DECK ERROR:
tacho sensor error

Recorder "error" LED flashing, not functional, enters STOP mode
Cause no output signal from one of the three tacho sensors (spooling motors, move sensor), or different sense of rotation of the three sensors, or no spooling motor tacho signal while the spooling motor supply current exceeds 4 A.
Action check ribbon cable connectors on the tacho sensors; check tacho sensors, replace if necessary; check the tape spindles as well as the move roller for free rotation
Priority 24

Display TAPE DECK ERROR:
tape tension incorr.

Recorder not functional
Cause difference between actual and nominal tape tension too large for more than one second
Action check the tape path and spindles for excessive friction
Priority 25

Display TAPE DECK ERROR:
radius measurm. err.

Recorder enters STOP mode
Cause computed radius of the tape rolls beyond permitted limits; tacho sensors defective
Action activate PLAY mode for several seconds (with tape). In general the error message disappears as soon as enough tacho pulses are present to compute the tape roll radii. Check tacho sensors, replace or repair
Priority 26

Display TAPE DECK ERROR:
communic. td-capst.

Recorder "error" LED flashing, enters STOP mode
Cause no data transfer via parallel interface of the Capstan Interface; Capstan Processor does not start up
Action replace Capstan Interface board
Priority 27

Display TAPE DECK ERROR:
pinch roller slipp.

Recorder "error" LED flashing, enters STOP mode
Cause pinch roller has excessive slip; capstan speed and tape speed do not correspond
Action clean pinch roller and capstan shaft; replace pinch roller if necessary; readjust pinch force correctly
Priority 28

Display TAPE DECK ERROR:
wrong inertia measu.

Recorder "error" LED flashing, enters STOP mode
Cause the three last computations of tape roll inertia did not produce admissible results
Action check all rollers and motors as well as the tape path for low friction
Priority 29

Display TAPE DECK ERROR:
bad capst. reference

Recorder "error" LED flashing, cannot reach requested nominal speed in PLAY or RECORD mode
Cause external varispeed reference is outside of admissible range, or missing; boards Master Serial Interface or Transformatter not connected; fault on one or both above mentioned boards; box-rack interconnection not established (backpanel rack or box, connectors on backside of tape transport)

Action correct or connect reference signal
Priority 30

Display

TAPE DECK ERROR: radius < max. hub

Recorder functional, tape guard function impaired, warning
Cause computed hub diameter diverges from the programmed value
Action set hub diameter according to actual value (alignment deck)
Priority 31

Display

TAPE DECK ERROR: radius > max. reel

Recorder functional, warning
Cause computed reel diameter diverges from the programmed value
Action reduce reel diameter
Priority 32

Display

TAPE DECK ERROR: move sensor hardware

Recorder "error" LED flashing, enters STOP mode
Cause move sensor board defective, or too many direction changes detected
Action replace, repair or readjust
Priority 33

Display

TAPE DECK ERROR: undefined error

Recorder "error" LED flashing, enters STOP mode
Cause unidentifiable error
Action switch mains voltage off and on; unplug RAM in Master MPU and reinsert it
Caution:
tape deck parameters lost, default values loaded! Either work with standard data, or reload stored parameters from tape, floppy disk or protocol; recalibrate recorder
Priority 1

Display

TAPE DECK ERROR: communication

Recorder "error" LED flashing, not functional
Cause software of Master MPU and Tape Deck MPU incompatible; fault on interface boards; no reply to status request
Action replace software; replace Master Serial Interface and /or Tape Deck Serial Interface
Priority 27

Display

AUDIO ERROR: no errors detected

Cause no errors detected during selftest
Action none

Display AUDIO ERROR:
initializing

Recorder not functional (except tape deck and Master MPU)
Cause Syscon initalization process not completed yet
Action switch mains voltage off and on; if error persists: change or repair Syscon board
Priority 40

Display AUDIO ERROR:
eprom checksum error

Recorder "error" LED flashing, may be functional
Cause error in Syscon EPROM (3 or 4 pcs.)
Action disconnect mains power and reconnect; change software
Priority 41

Display AUDIO ERROR:
ram read/write error

Recorder "error" LED flashing, "error" is indicated in the secondary keyboard, recorder frozen, enters STOP mode
Cause RAM-test failed, defective RAM
Action replace RAM
Priority 42

Display AUDIO ERROR:
battery voltage

Recorder "error LED flashing, functional, non-volatile status may have been lost at power-down
Cause battery voltage low
Action replace battery in Syscon board (box)
Priority 43

Display AUDIO ERROR:
sysbus error

Recorder "error" LED flasing, not functional
Cause short circuit and/or Sysbus driver/receiver failure
Action remove all boards connected to Sysbys except System Controller (consult vol. III of D820X manuals, section "Commands Syscon-Hardware", par. "overview of device address assignment"); insert sequentially
Priority 44

Display AUDIO ERROR:
timing error

Recorder "error" LED flashing, "error" is indicated in the secondary keyboard, recorder frozen, enters STOP mode
Cause self-test error on Timing + Test board (signal /TTERROR/)
Action replace or repair Timing + Test board located in PCM box
Priority 45

Display AUDIO ERROR:
nonvolatile status

Recorder "error" LED flashing, "error" is indicated in the secondary keyboard, recorder frozen
Cause communication checksum error between Master MPU and Syscon; block checksum calculation failed
Action press STORE; switch mains voltage off and on
Priority 46

Display AUDIO ERROR:
unusual reset

Recorder functional
Cause unusual power-down, actication of reset button on Syscon board
Action press STORE; when Display panel not active: disconnect mains power and reconnect or press reset button on Master MPU
Priority 47

Display AUDIO ERROR:
check timing board

Recorder "error" LED flashing, not functional
Cause missing or defective Timing + Test board
Action replace or repair Timing + Test board
Priority 48

Display AUDIO ERROR:
check gains cntr brd

Recorder "error" LED flashing, not functional
Cause missing or defective Gains Control board
Action replace or repair Gains Control board
Priority 49

Display AUDIO ERROR:
check detector board

Recorder "error" LED flashing, not functional
Cause missing or defective Detector board located in cage behind headblock
Action replace or repair Detector board
Priority 50

Display AUDIO ERROR:
check pdm board

Recorder "error" LED flashing, functional, except cue tracks
Cause missing or defective PDM Modulator board located in rack
Action replace or repair PDM Modulator board
Priority 51

Display AUDIO ERROR:
check rt/tc board

Recorder "error" LED flashing, functional, except RECORD mode, no time code recording and/or reproduction
Cause missing or defective RT/TC Codec board located in PCM box
Action replace or repair RT/TC Codec board
Priority 52

Display AUDIO ERROR:
check monitor board

Recorder "error" LED flashing, functional, except built-in Monitor panel or Tape Deck Monitor
Cause missing or defective Monitor panel located in penthouse, or Tape Deck Monitor board located in cage behind headblock (versions without penthouse only)
Action replace or repair Monitor panel or Tape Deck Monitor board
Priority 53

Display AUDIO ERROR:
PLL out of range

Recorder "error" LED flashing, not functional (muting)
Cause VCXO-PLL: lock not achieved; applied external reference frequency outside of admissible range (see par. 1.7, interfacing specifications), or missing; VCXO board or Timing + Test board defective
Action check signal /TTLOCK/ (R_80_B, bit 2), should be logical high when out-of-lock; correct or connect external reference frequency; repair or replace VCXO or Timing + Test board located in PCM box
Priority 54

Display AUDIO ERROR:
override disabled

Recorder functional
Cause recorder reacts to information in DI, RT or data blocks concerning sampling rate and/or emphasis setting. Any attempt to change states (sampling frequency or emphasis) that are specified as override disable, is ignored; message may also appear during single channel recording (see keys 018, INPUT: DIGITAL/ANALOG and 019, EMPHASIS: ON/OFF, or par. 2.5.7, Record)
Action none, key setting ignored
Priority 55

Display AUDIO ERROR:
auto mode disdabled

Recorder "error" LED not flashing, functional (message appears with Extended Syscon 1.861.764 only)
Cause attempt to deliberately ignore one or more of the auxiliary track flag settings from the reference time track, to either overwrite modulated or unmodulated TC or CUE track(s), or to neglect the flag for AUX3 setting (data or cue)
Action restore condition requested by reference time track as soon as possible
Priority 56

Display AUDIO ERROR:
check external sync

Recorder "error" LED flashing, not functional
Cause external synchronization signal out-of-range or missing (see par. 1.7, interfacing specifications)
Action restore requested condition
Priority 57

Display AUDIO ERROR:
no reference track

Recorder "error" LED flashing, functional, except RECORD mode; enters STOP from RECORD mode
Cause PLAYBACK:
reference track missing, no DASH tape, different DASH version used during recording (e.g. DASH-S, 7.5 ips.),
RECORD:
incorrect recording current, connector to write head not inserted, defective playback electronics, defective Write Amplifier, defective RT/TC Codec board
Action replace tape, check recording and playback conditions (watch CRC error LED on board RT/TC Codec), replace or repair above mentioned boards
Priority 58

Display AUDIO ERROR:
rt fs not available

Recorder "error" LED flashing, not functional (wrong speed and sampling frequency)
Cause sampling frequency specified on reference time track not installed
Action replace VCXO board or Timing + Test board located in PCM box
Priority 59

Display AUDIO ERROR:
rt fs unspecified

Recorder "error" LED flashing, functional enters default value (48 kHz sampling frequency)
Cause sampling frequency not specified in reference time control word (pattern 000)
Action check with "show status" diagnostic screen (RT info), try to identify correct sampling frequency by toggling sampling frequency key, press STORE
Priority 60

Display AUDIO ERROR:
illegal rt format

Recorder "error" LED flashing, not functional, erroneous playback of digitalaudio data
Cause check of twin flag and/or format version indicated in reference time failed
Action tape can not be reproduced (format mismatch)
Priority 61

Display AUDIO ERROR:
illegal di format

Recorder "error" LED flashing, functional, no control via DI
Cause check of bit 0 in byte 00 of digital input (DI) status word failed
Action none, recorder reacts to bit 3 (emphasis) only, no control via keyboard of sampling frequency and emphasis
Priority 62

Display AUDIO ERROR:
di fs not available

Recorder "error" LED flashing, not functional (wrong speed and sampling frequency)
Cause sampling frequency specified via digital input status word not installed
Action replace VCXO board or Timing + Test board located in PCM box
Priority 63

Display AUDIO ERROR:
di fs unspecified

Recorder "error" LED flashing, functional, enters default value (48 kHz sampling frequency)
Cause bits 6 and 7 of digital input (DI) status word set to 00
Action check with "show status" diagnostic screen (DI info), try to identify correct sampling frequency by toggling sampling frequency key, press STORE
Priority 64

Display AUDIO ERROR:
di emph not avail.

Recorder "error" LED flashing, functional
Cause specified emphasis type (CCITT J17) not installed
Action recorder is transparent in STOP and INPUT mode, but not transparent in RECORD mode; correct output of DO status word not possible
Priority 65

Display AUDIO ERROR:
rt fs mismatch

Recorder "error" LED flashing, functional
Cause manual override error, key setting not according to reference time control word
Action correct key setting (sampling frequency)
Priority 66

Display AUDIO ERROR:
tape emph mismatch

Recorder "error" LED flashing, functional
Cause manual override error, key setting not according to information contained in digitalaudio data blocks (e.g. during channel sequential recording)
Action correct key setting (emphasis)
Priority 67

Display AUDIO ERROR:
di fs mismatch

Recorder "error" LED flashing, functional, wrong tape speed
Cause status word of digital input (DI) does not match reference time control word regarding sampling frequency in PLAY mode
Action change content of source status word, or change tape
Priority 68

Display AUDIO ERROR:
di emph mismatch

Recorder "error" LED flashing, functional
Cause attempt to set emphasis incorrect ignored; the recorder detected that a mismatch would exist between the emphasis setting on tape (as written in the data blocks) and the requested setting from digital input during channel sequential recording (single channel record)
Action change source status word according to tape regarding emphasis
Priority 69

Display AUDIO ERROR:
communication

Recorder "error" LED flashing, not functional
Cause communication Syscon-Master defective, software of Syscon and Master MPU incompatible, no reply to status request, board Master-Syscon Interface (located in rack) defective or not inserted
Action replace or repair board Master-Syscon Interface, replace software
Priority 10

2.8 Editing

2.8.1 Tape Cut Instructions

Cleanliness is the mandatory rule for successful splicing of digitally recorded tapes. Although the D820X utilizes a very strong error correction code and has been built to recognize splices under nearly all circumstances, it may be useful to remember that 1500 bits are recorded per millimeter of tape due to the high packing density of the DASH format. In case of a dust particle of less than 1 millimeter, more than 5 blocks are invariably destroyed, because distance losses are always involved. Therefore
Make sure that your working environment is as clean as possible and that fingerprints on the tape are reduced to an absolute minimum!

Here are the nine golden rules for successful tape-cutting:

- Clean the tape deck and especially the splicing block with alcohol. Kaltron is recommended for head cleaning.
- Wash your hands to remove grease and dirt.
- Mark the tape with an appropriate pen (see recommendation in par. 1.5) and extend the portion to be cut out by 1.7 mm on both sides to make sure that the section will be inaudible.
- Use scissors for the splicing tape and clean and sharp blades for the tape itself. Refer to par. 2.5.24 for cutting with the built-in scissors.
- Allow for a very small gap between the two tape ends (approximately 0.1 mm). Always cut at right angle to the tape edge. Do never allow for the ends to overlap!
- Do not touch the tape within a distance of less than 50 mm from the splicing area. Recognizing splices is impaired in erroneous sections (many block errors due to fingerprints).
- Apply short pieces (length 20 to 30 mm) of thin splicing tape (see recommendation in par. 1.5) onto the audio tape. Cut the ends of the splicing tabs at an angle of approximately 60 degrees. Apply from one side to the other and rub gently. Do not allow for air bubbles or dust particles in and on the splicing tabs.
- Make sure that the splicing tape does not protrude the audio tape; both should be parallel to each other. Otherwise distance and azimuth losses occur.
- Do not attempt to remove the splicing tape if correction is required within distance of less than the length of the splicing tape. Cut through the audio and splicing tape and apply a new splicing tape over the old.

Note: It is recommended to clean tapes from fingerprints, oil, etc. with aethylene alcohol, containing aproximately 30 % alcohol. Let ample time for the fluid to dry, because wet tapes tend to stick together.

Splicing with leader tape:
Leader tape may be inserted directly in front of a tape containing an audio section. No synchronizing signals are needed for the capstan servo in front of the audio event, because the recorder will operate at nominal speed when no data is detected and the time required to adjust to the exact speed (when data is read again) is compensated for in the time base corrector. Approximately 100 msec. is needed to verify incoming block sync words and to demute the audio path. This is the time by which the leader tape will be elongated. Normally the recorder performs a fade-in of 9 blocks (4.5 msec. at 48 kHz sampling rate) for the digital audio signals.

Electronic splice handling:
At the splicing point, an electronic crossfade (crossfiltering in the D820X) takes place with a total length of 18 blocks (duration of 1 block: 0.5 msec.).

One of the most critical factors concerning tape cutting is the detection of splices in an erroneous zone. The D820X uses elaborate techniques for this purpose:

- The occurence of block sync patterns within a certain time window is evaluated for all eight tracks.
- The block numbers are checked for discontinuities.
- The P and Q correction lines constantly check for interleave errors.
- The sudden appearance of a so called CRC-gap (a burst of block errors on all tracks) may also indicate a splicing point.

In the D820X splice detection is completely independent of the reference time track. When RT SYNC is selected interleave errors only are used to detect splices.

Splice constraints:

A Minimum length of tape to be cut out for the event to become inaudible: 18 blocks (3.429 mm).
B Distance, of which a cut-out piece of tape should be elongated: 9 blocks at both ends. Otherwise it may become audible in the crossfade area (2 * 9 blocks).
C Minimum distance before a new splice can be processed: 187 blocks.
D Minimum distance between splices for (theoretically) full correction: 221 blocks.

In practice is is advisable to maintain a distance of 4.7 cm between splices, as indicated on the splicing block.

1 block corresponds to 0.5 msec. or 0.1905 mm

(valid for 48 kHz sampling frequency)

Note: due to the constraints **A** and **B** above a varible crossfade time could become difficult to handle for the operator and has been omitted therefore. Constraint **D** has been carefully optimized. Other recorders may need an interval of 500 blocks between edits.

The D820X has full error correction capabilities due to the twin recording format. No interpolation is necessary when data on tape is in good condition because all samples will be available over the crossfade region.
Playback performance of poor splices may be improved by selecting RT SYNC mode.

2.8.2 Electronic Splicing

The operation is also called punching, overdubbing, dropping in and out, etc. It refers to overwriting sections of tape in single or multichannel mode. When single channel operation is required, RT SYNC mode should be selected for reliable servo and data synchronizer control (par. 2.5.8). The D820X performs "hard punches" when recording is activated over a previously written section. This means that the new section appears suddenly (without crossfade) and at arbitrary locations on tape. In order to minimize the destroyed area, the write amplifier is enabled at block edges only. Even then, at least one block of data will most certainly become unreliable.
The recorder treats electronic splicing identical as mechanical splicing: it performs crossfade operations (crossfiltering in the D820X) at the punch-in and -out points during playback. Electronic splicing is in all respects identical to mechanical splicing for the recorder, except that less data is destroyed and that recognizing the splicing point is more reliable therefore.
Two of the constraints which apply to mechanical tape cutting are to be considered with electronic splicing too:

- minimum distance before a new splice can be processed: 187 blocks. Otherwise the information in-between is muted.

- minimum distance between splices for (theoretically) full correction: 221 blocks. When the distance is between 187 and 221 blocks second or first order interpolation is necessary.

In practice it is advisable to maintain a distance of 4.7 cm between splices, as indicated on the splicing block.

1 block corresponds to 0.5 msec. or 0.1905 mm

(valid for 48 kHz sampling frequency)

2.8.3 Operation with Electronic Editors

The D820X is optimized to interface with the STUDER Electronic Editor DE4003 and the STUDER-PHILIPS PQ-Editor LHH 3050. The operation is described in the manual supplied with the editors.
The Electronic Editor requires RT SYNC mode to perform punch-in/-out and append operations without splice detection and corresponding crossfiltering. The DE4003 therefore initializes with RT SYNC enabled. In order to append already existing recordings into a blank tape area the commands APE and APD are available via serial port only. Command APE (append enable) together with RECORD performs normal record operation. Splice detection, however, is different because the occurence of block syncs within a certain time window and discontinuities of block addresses (see par. on "electronic splice handling" above) are not considered. Appends (and punch-in's) are normally placed less accurate regarding block sync distances than in normal RECORD mode of the recorder. Command APE together with RECORD thus enables appending recordings without splice detection.
Due to reasons of audio and control interfacing and of delay and blocking structures, etc., interfacing editors from other manufacturers is not supported.

2.9 Daily Care

2.9.1 Cleaning

Daily care is limited to cleaning of the heads, the capstan shaft, the tape guidance elements and all surfaces of the tape transport that come in direct contact with the magnetic tape (e.g. the splicing block) and with the self-adhesive splicing tape. Head cleaning is best performed with Kaltron 113 MDR, available through STUDER representatives. Anti-static screen and terminal wipes as available for computer equipment (Electrolube "Safeclens", etc.) may be used with care. To clean the transport, a general purpose nondetergent household cleaner is sufficient.

2.9.2 Demagnetizing

It is strongly recommended not to demagnetize the heads!

Inadequate demagnetizers (Handymag, etc.) may easily have a detrimental effect. The D820X has been shipped with carefully demagnetized heads. It will work even with magnetized heads without increased block error rate due to the adaptation process built into the playback circuitry. The heads, however, may magnetize the tapes and recorders with inferior playback circuitry exhibit a higher error rate. This could cause compatibility problems. It is therefore recommended to check the error rate of the recorder frequently by applying the following procedure:

- use a virgin tape of a manufacturer recommended by STUDER.
- select REFERENCE EQ TABLE in the alignment audio menu and 48 kHz sampling frequency. When the REFERENCE EQ TABLE is active, the adaptation process is stopped. Equalization is performed with the built-in standard ROM table, made for an "average" head and playback circuitry and an "average" tape (actually the IEC digital audio primary reference tape from AMPEX, production no. 8000).
- make a first recording and monitor the block error rate during 50 seconds (which corresponds to 10**5 blocks at 48 kHz). There are several methods by which this can be performed. The most convenient and least accurate way is to watch the 8 LED on the Transformatter board located in the PCM box. With some experience this method may be adequate. A better way is to count CRC errors in "show quality" mode. It requires a terminal or a computer connected to the "test" connector at the PCM box and can be performed on a track by track basis. Another possibility may be to use a STUDER CRC Checker (1.861.991). Both latter methods are accurate and reliable. For more information see par. 3.4 (servicing displays on boards)
- overwrite the first recording during at least 50 seconds and monitor the block error rate again over 50 seconds. Make sure that pinch roller activations are outside those 50 seconds.
- the block error rate for steps 3 and 4 should not increase 50 per track, which corresponds to 500 ppm. Approximately identical results should be obtained for multiple measurements of the same piece of tape.
- when the block error rate is above 500 ppm per track and fluctuates heavily, the recording currents may not be optimally adjusted, or the read head may be magnetized. Refer to par. 3.5, Service Adjustments, to set the recording currents, or, in the latter case, contact your nearest STUDER representative for further information.

When a very powerful degausser is at disposal, proceede as follows: turn off the power switch of the D820X. Move the demagnetizer from a distance of ca. one meter slowly to

one of the heads after it has been switched on. Circular or up and down motions should be carried out as close as possible in front of each head without touching the head surface, and then pulled away very (!) slowly, until a distance of at least one meter is reached between the demagnetizer and the head. The reason for this is that the transformers connected to the read head can be magnetized if the distance is to small. When a demagnetizer with a very strong field is used, it may be necessary to disconnect the transformers from the read head. For this, the cover of the headblock and the screening assembly below must be removed.

2.9.3 Tape Tension and Recording Current

It may be advantageous to check the tape tension and record current settings (alignment audio and alignment deck menu). The tension figures should correspond to those indicated in the individual Test Report supplied with each recorder. The current settings for tape A and B should be set to zero unless a recommendation to accomodate a vastly different tape formula is issued by STUDER.
Par. 3.5 (service adjustments) contains more information regarding tape tension adjustments.

2.9.4 Capstan Motor

The capstan motor is carefree; to increase its service life, lubricating the capstan bearing once a year is recommended. For this purpose, apply one drop of oil (type PDP 65, order no. 20.020.401.04).

2.10 Operation with Serial Interface

Two different interface types are available:
Version 1.810.751 is designed for operation with terminals, computers and controllers according to RS-232, ASCII format, or for storing the audio parameters for backup purposes on an external storage medium such as floppy or hard disks. Version 1.820.751 is designed for operation with terminals, computers and controllers according to RS-232, binary format, or for connection to an ES (SMPTE/EBU) bus.

2.10.1 SMPTE/EBU-BUS (ES-BUS)

The SMPTE/EBU bus (ES bus) is a sophisticated control facility permitting interconnection of several individual units to form a flexible and powerful system (for example remote control of several recorders).

2.10.2 Data Backup with Personal Computer

For copying audio and tape tension parameters of the RAM to an external storage medium, the tape recorder must be equipped with serial interface 1.810.751. Data can be stored on a floppy or hard disk installed in a personal computer.
External data can be compared with data stored in RAM of the recorder in order to check data transfer. The expressions SAVE (for external storage of the recorder's RAM data), VERIFY (for comparing externally stored data with those in the recorder's RAM), and LOAD (for writing externally stored data into the recorder's RAM) are used below.

2.10.2.A **Storing the Parameters on a Personal Computer (SAVE)**

If the recorder receives the command "SAVE" from the keyboard, the microprocessor transfers all stored audio and tape tension parameters in serial format to the SMPTE/EBU BUS / RS232 connector. Three complete copies of the parameters are transmitted each time for safety reasons.

Procedure:

- Putting the personal computer into operation and connecting it to the SMPTE/EBU BUS / RS232 connector:
  As described in 2.8.5. In addition, the software handshake mode (X ON/X OFF protocol) must be switched on.
- Bring the programming enable switch [28] to its counterclockwise end position (with Allen key No. 2.5).
- Press ↓/NEXT several times until the service display shows the following menu:

  ```
  PARAM BACKUP RS 232
  ↑_↓ VERIFY SAVE LOAD
  ```

  The cursor is between the two arrows in a safe position.
- Press →/CURSOR two times, the cursor stands now below the word "SAVE".
- Press STORE, the service display shows:

  ```
  DATA TRANSMISSION IN
  PROGRESS - PLS WAIT
  ```

  The data are transmitted to the computer.

- After a successful data transmission, the following message appears:

```
DATA TRANSMISSION
  COMPLETED
```

The transmitted data can be stored on the floppy disk.

- If data transmission errors have occurred (e.g. caused by a transient system voltage failure), the following message appears:

```
DATA TRANSMISSION
   FAILED
```

- Pressing ↑/NEXT or ↓/LAST switches over in both cases to the following menu:

```
PARAM BACKUP RS 232
↑_↓ VERIFY SAVE LOAD
```

- If required, the procedure can be repeated. If not, page back to the starting position by pressing ↑/LAST several times.

Verification of the data in the Personal Computer (VERIFY)
If the tape recorder receives the command "VERIFY" from the keyboard, the microprocessor expects all audio and tape tension parameters in serial format from the SMPTE/EBU BUS / RS232 connector.

Procedure:

- Putting the personal computer into operation and connecting it to the SMPTE/EBU BUS / RS232 connector:
  As described in 2.8.5. In addition, the software handshake mode (X ON/X OFF protocol) must be switched on.
- Bring the programming enable switch [28] to its counterclockwise end position (with Allen key No. 2.5).
- Press ↓/NEXT several times until the service display shows the following menu:

```
PARAM BACKUP RS 232
↑_↓ VERIFY SAVE LOAD
```

The cursor is between the two arrows in a safe position.

- Press →/CURSOR once, the cursor stands now below the word "VERIFY".
- Press STORE, the service display shows:

```
WAITING FOR DATA INP
PLS SEND DATA
```

- activate data transmission from the personal computer to the tape recorder. As soon as valid data is recognized, the service display indicates:

```
VERIFYING DATA
 PLEASE WAIT
```

- After successful data comparison, the following message appears:

```
VERIFICATION SUCCESSFULLY
   COMPLETED
```

- If data is not identical, the following message appears:

```
VERIFICATION FAILED
  PLEASE REPEAT
```

- The following message appears:
  after about 15 seconds, if no data transmission took place, or
  after about 30 seconds, if no valid data could be found:

```
NO DATA FOUND
```

- In all cases, pressing ↑/LAST switches back to the following menu:

```
PARAM BACKUP RS 232
↑_↓ VERIFY SAVE LOAD
```

- If required, the procedure can be repeated. If not, page back to the starting position by pressing ↑/LAST several times.

Loading data from the Personal Computer (LOAD)
If the recorder receives the command "LOAD" from the keyboard, the microprocessor receives all audio and tape tension parameters in serial format an loads them into RAM. Generally, the first of the three identical data blocks is sufficient for the LOAD procedure. If errors should occur during LOAD, the microprocessor can read from one of the two following data blocks.

Procedure:

- Analogous to 4.8.5, until the following menu is indicated:

```
PARAM BACKUP RS 232
↑_↓ VERIFY SAVE LOAD
```

- Press →/CURSOR three times, the cursor stands now below the word "LOAD".
- Press STORE, the service display shows:

```
WAITING FOR DATA
 PLS SEND DATA
```

- Activate data transmission from the personal computer to the tape recorder. As soon as valid data is recognized, the service display indicates:

```
DATA LOADING IN
PROGRESS - PLS WAIT
```

- After successful data loading, the following message appears:

```
  DATA LOADING
   COMPLETED
```

- If the microprocessor detects a data error (e.g. caused by a transient system voltage failure), the following message appears:

```
DATA LOADING FAILED
DEFAULT PARAM LOADED
```

Repeat the procedure, or, if requested, proceede working with standard (default) parameters.

- The following message appears:
  after about 15 seconds, if no data transmission took place, or
  after about 30 seconds, if no valid data could be found:

NO DATA FOUND

The previous audio and tape tension parameters are still present in RAM.

- In all cases, pressing ↑/LAST switches back to the following menu:

PARAM BACKUP RS 232 ↑_↓ VERIFY SAVE LOAD

- If required, the procedure can be repeated. If not, page back to the starting position by pressing ↑/LAST several times.

The following message appears:

VERIFICATION SUCCESSFULLY COMPLETED

2.10.3.A

RS-232 Interface

The term "RS-232" defines an interconnection process between two devices (point-to-point link). The standard defines:

- electrical characteristics (level, lines),
- mechanical characteristics (connectors),
- signal descriptions, and
- standard connections.

The interface operates with data rates up to 20 kbit/s and cable lengths of up to 15 m. The signal levels are defined as follows:

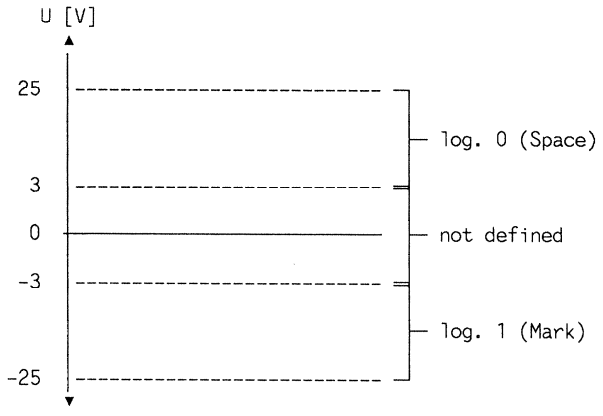
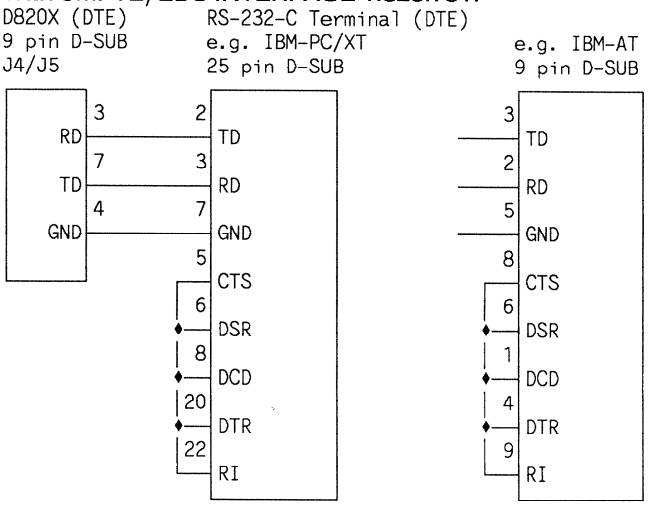
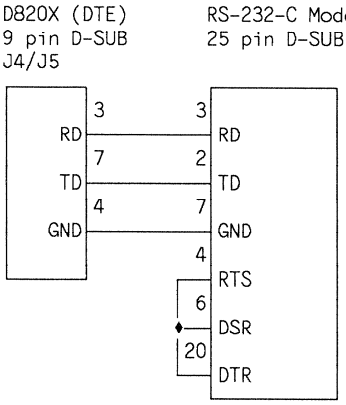


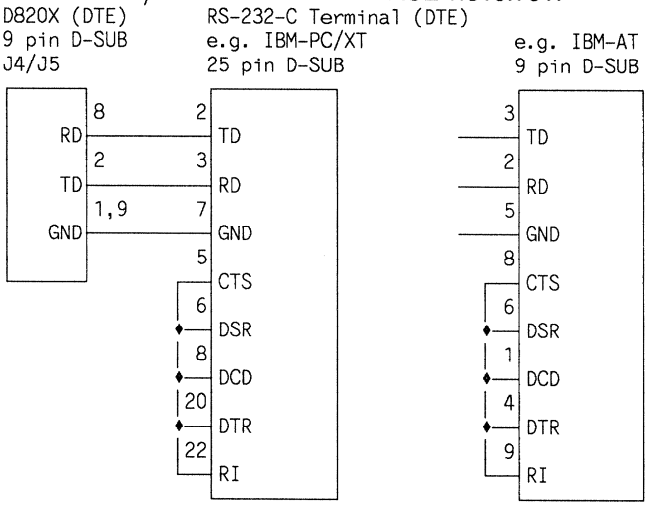
Fig. 2.10.3 below shows three examples for interfacing the D820X with a) an IBM-XT personal computer, or b) an IBM-AT personal computer and c) a modem.

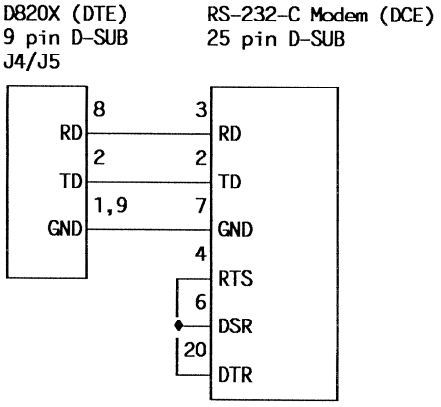
With SMPTE/EBU INTERFACE 1.820.751:





With RS-232/DATA SAVE INTERFACE 1.810.751:





For more information see chapter 2.10.5 and 2.10.6 below.

2.10.3.B **RS-422 Interface**

To be defined.

2.10.4 ASCII Interface

The purpose of the interface:
It is used to interconnect synchronizers, audio editors (DE 4003), personal computers, the PQ-editor and other devices with the D820X. Control information only is transmitted and received via this interface.
The serial interface of the D820X uses a 9-way connector according to SMPTE instead of a 25-way connector. The user can decide by means of an adapter cable whether the unit is to be a terminal or a modem.

Recorder 9-pin		Terminal 25-pin		Modem 25-pin	
Signal	Pin No.	Signal	Pin No.	Signal	Pin No.
SNDATA	2	Trans.Data	2	Trans.Data	3
RCVDATA	8	Rec. Data	3	Rec. Data	2
GROUND	9	Sig. Ground	7	Sig. Ground	7

No additional handshake lines are used. A software handshake (X ON/X OFF protocol) is implemented for all baud rates, however only required for 9.6 kbaud.
X ON = 0001 0001 (ASCII DC1) = continue
X OFF = 0001 0011 (ASCII DC3) = interrupt
After reception of X OFF the recorder transmits no more than 2 additional characters. After the recorder has transmitted X OFF, it can still receive five characters without losing an instruction.
The following data is fixed:
1 Start bit
1 Stop bit
8 Data bits
No parity bit.
The following baud rates can be set: 300, 1200, or 9600.
Only ASCII characters are accepted as data.

2.10.5 Operation of the ASCII Interface

- Configuration of terminal or personal computer (e.g. call program VTERM in IBM personal computers):

Communication rate:	300, 1200 or 9600 (*)
Bits per character:	EIGHT (**)
Parity:	OFF
Stop bits:	ONE
Auto xon/xoff:	ON (data buffer overflow)
Local echo:	OFF

(*) according to ASCII RS-232 Baud Rate setting in the Alignment Deck menu
(**) according to BIN RS-232/422 FORMAT setting in the Alignment Deck menu
Connect handshake lines CTS and RTS to "low".

- Set the configuration of the recorder accordingly (remarks *, **).
- SERIAL REMOTE CONTROLLER 1.810.751: the board contains receiver and driver for the STUDER interface used for data backup with a personal computer (PC), and the RS-232 interface. Select the appropriate mode by means of jumper JS1. Jumper in position X: set switch no. 2 of SZ1 (DIL switch on top) to OFF for RS-232 communication.
  Jumper in position H: software controlled switchover between STUDER bus and RS-232. Normally, the jumper should be in position H.

Insert PCB SERIAL REMOTE CONTROLLER; switch the LED monitor on with DIL switch no. 1 of SZ1 (DIL switch on top); both LED's RX and TX are illuminated as long as no interconnection is established.

- Connect the personal computer or the terminal with an adapter cable to one of the nine way connectors labeled "SMPTE/EBU BUS" and "RS-232". If the transfer works, both LED's RX and TX become dark.
- After a reset or power-up/down the screen indicates

  Welcome to the
  D820X MASTER Monitor
  REL ww/yy (C) PCM SoftTeam
  STUDER AG CH-8105 REGENSDORF

  Monitor for xxxxxxx Terminal

- Type "echo on". Note that for synchronizer mode the echo mode is set to off each time key SYNCHRONIZER ON is activated. Default value for synchronizer is ON. Therefore after each power-up the echo mode has to be selected again (type ECHO ON).
- Select the appropriate terminal type by entering TYPE and a list of implemented terminal drivers appears.
- Now the desired commands (see list below) can be entered via keyboard. Commands are executed after having pressed ENTER or LINE FEED, respectively.
- Enter H for HELP to get a list of available instructions. The list can be stopped and started by pressing any key.
- For more information on the Master Monitor see section 3 in volume III of the D820X manuals.

Instruction Set

Note: optional statements are denoted with [ ], obligatory statements with ◄ ►

ABBREV.	INPUT	OUTPUT	DESCRIPTION
LCD	LCD [,:] CR	CR,LF	Local keyboard disabled
LCE	LCE [,:] CR	CR,LF	Local keyboard enabled
RMD	RMD [,:] CR	CR,LF	Remote keyboard disabled
RME	RME [,:] CR	CR,LF	Remote keyboard enabled
STP	STP [,:] CR	CR,LF	Function stop of tape deck
PLY	PLY [,:] CR	CR,LF	Function play of tape deck
FWD	FWD [,:] CR	CR,LF	Function forward of tape deck
WNF < >	WNF <xxxx> CR (0 <=xxxx<= 5FFF) 5FFFH=15.73 m/sec	CR,LF	Forward with selected speed (x[dec]/1563 = a m/sec) 1 m/sec = 061BH
RWD	RWD [,:] CR	CR,LF	Function rewind of tape deck
WNR < >	WNR <xxxx> CR (0 <=xxxx<= 5FFF) 5FFFH=15.73 m/sec	CR,LF	Rewind with selected speed (x[dec]/1563 = a m/sec) 1 m/sec = 061BH
EDI	EDI [,:] CR	CR,LF	Function edit of tape deck
REC	REC [,:] CR	CR,LF	Function record of tape deck
STM < >	STM <(-)hh[,:]mm [,:]ss[,:]xxx> CR with x=ms	CR,LF	Set timer at address < > with -10<hh<24, -1<mm<100, -1<ss<100, -1<xxx<1000 and -10hours < address < 24hours
TID	TID [,] CR	CR,LF	Display time in the LED displ.
WAD	WAD [,] CR	CR,LF	Display watch in the LED disp.
RTD	RTD [,] CR	CR,LF	Display rt in the LED display
TCD	TCD [,] CR	CR,LF	Display tc in the LED display
TM?	TM? [,:] CR	(-,h)h:m m:ss:xxx CR,LF	Timer ? show the value from the actual LED display indication
LOC < >	LOC <(-)hh[,:]mm [,:]ss[,:]xxx> CR with x=ms	CR,LF	Locate to address < > with -10<hh<24, -1<mm<100, -1<ss<100, -1<xxx<1000 and -10hours < address < 24hours
LMV < >	LMV <xxxxxxxx> CR with xx=1 byte	CR,LF	Wind to counter address < >
MV?	MV? [,:] CR	xx xx xx xx CR,LF	Show state of move roller counter with xx : 1 byte
REA (i)	REA (i) [,] CR i=1,2,3,4,F	CR,LF	Set channel i to ready 1,2 : CH1, CH2 3 : TC 4 : AUX (in AUX4MIX) F : all above
SAF (i)	SAF (i) [,] CR i=1,2,3,4,F	CR,LF	Set channel i to safe 1,2 : CH1, CH2 3 : TC 4 : AUX (in AUX4MIX) F : all above

ABBREV.	INPUT	OUTPUT	DESCRIPTION
INP (i)	INP (i) [,] CR i=1,2,3,4,F	CR,LF	Set channel i to input 1,2 : CH1, CH2 3 : TC 4 : AUX (in AUX4MIX) F : all above
REP (i)	REP (i) [,] CR i=1,2,3,4,F	CR,LF	Set channel i to repro 1,2 : CH1, CH2 3 : TC 4 : AUX (in AUX4MIX) F : all above
RTN	RTN [,:] CR	CR,LF	Rt sync enabled
RTF	RTF [,:] CR	CR,LF	Rt sync disabled
SBA < >	SBA <xxxx> CR	CR,LF	Set ES bus address (two lower bytes min is 80H and two higher bytes min is 82H)
BA?	BA? [,:] CR	xxxx CR,LF	Show ES bus address
MSN	MSN [,] CR	CR,LF	Master safe enabled
MSF	MSF [,] CR	CR,LF	Master safe disabled
SAP < >	SAP <i,j,x.y> CR with i=1,2 j=0,I -.1<x.y<20.1	CR,LF	Set analog levels (line level j / i: x.y dBm) (O: output, I: input)
SPF < >	SPF <x> [,] CR x=0,4,6,8,10,15, 20 dBm	CR,LF	Set analog levels fixed (line level x dBm for all channels)
SDO	SDO [,] CR	CR,LF	Set digital gain 0 dB for all channels
SDG < >	SDG <i,j,(-)x.y> CR with i=1,2 j=0,I and -10.1<x.y<6.1	CR,LF	Set digital gain j / i: x.y dB (O: output, I: input)
CUL < >	CUL <i,x.y> CR with i=1,2 -0.1<x.y<20.1	CR,LF	Set cue level(s) channel i i: 1,2 ; x.y dBm
GA? < >	GA? <i,j> CR with j=ia,oa, id,od,cu and i=1,2	xx CR,LF	Gain ? ia = input analog oa = output analog id = input digital od = output digital cu = cue
SAI <j>	SAI <j> [,] CR with j=m,a	CR,LF	Set autoinput j m = mute a = auto
AMU <j>	AMU <j> [,] CR with j=y,n	CR,LF	Automute yes or no
MAN	MAN [,] CR	CR,LF	Mute both main channels (soft mute), CH1, CH2
MAF	MAF [,] CR	CR,LF	Demute both main channels (soft demute), CH1, CH2
AED <j>	AED <j> [,] CR with j=y,n	CR,LF	Autoedit yes or no

ABBREV.	INPUT	OUTPUT	DESCRIPTION
DAI <j>	DAI <j> [,] CR with j=a,d	CR,LF	Set digital or analog input
EMP <j>	EMP <j> [,] CR with j=y,n	CR,LF	Emphasis yes or no
SSR <p>	SSR <p> [,] CR with p=hi,lo	CR,LF	Set sampling rate to p rate; HI, LO as configured on D820X
AA4 <p>	AA4 <p> [,] CR with p=mix,cue	CR,LF	Assign aux4 to mix or cue
RCU <j>	RCU <j> [,] CR with j=ana,auto	CR,LF	Reproduce cue track(s) ana = repro of bias recordings auto= according to flag on rt
HPF <j>	HPF <j> [,] CR with j=y,n	CR,LF	High pass filter on yes or no
IPC <p>	IPC <p> [,] CR with p=int,ext, bal,unbal	CR,LF	Sync input intern,extern,balanced or unbalanced (composite video)
OPC <p>	OPC <p> [,] CR with p=sec,wor	CR,LF	Output clock sector or word
IPT <p>	IPT <p> [,] CR with p=vid_ebu, ntsc_bw, ntsc_col, syn, wcl	CR,LF	Input video ebu, video ntsc bw, video ntsc col, synchronizer or word clock
SRH	SRH [,] CR	CR,LF	Rehearsal mode enabled (EE2) Stereo operation only
CRH	CRH [,] CR	CR,LF	Rehearsal mode disabled (EE2) Stereo operation only
EED	EED [,] CR	CR, LF	Any connected EE loop disabled
EEL	EEL [,] CR	CR, LF	EE loop 1 (left) enabled
EER	EER [,] CR	CR, LF	EE loop 1 (right) enabled
EE1	EE1 [,] CR	CR, LF	EE loop 1 enabled (both CH)
VDM <p>	VDM <p> [,] CR with p=%,ips,ht	CR,LF	Set varispeed display mode %, inch per second or half tone
VEN	VEN [,] CR	CR,LF	Varispeed enabled
VEF	VEF [,] CR	CR,LF	Varispeed disabled
SVS < >	SVS <(-)x.y> CR with -12.6<x.y<12.6	CR,LF	Set varispeed x.y %
LFT	LFT [,] CR	CR,LF	Lifter enabled
EDT	EDT [,] CR	CR,LF	Lifter disabled
FEN	FEN [,] CR	CR,LF	Fader start ready key enabled
FEF	FEF [,] CR	CR,LF	Fader start ready key disabled
ROL <p>	ROL <p> CR with p=s,p,r	CR,LF	Set rollback stop, play or record
FRA <p>	FRA <p> [,] CR with p=25,29.97, 30	CR,LF	Set time code delay to p frames per second

ABBREV.	INPUT	OUTPUT	DESCRIPTION
DIS <p>	DIS <p> [,] CR with p=co,usr, una	CR,LF	Select display of code, user bits or unassigned bits
ST?	ST? [,] CR	xx CR,LF	Status equates ? see list of STATUS EQUATES
MS?	MS? [,] CR	xx CR,LF	Messages from syscon 76543210 ||`-> VCXO locked, TTLOCK |`--> PLL locked, RANGEOK `---> digital input lock.
SO?	SO? <x> [,] CR	xx CR,LF	Display of status. For x see POSITION in list DISPLAY OF STATUS.
DST	DST [,] CR	(-,h)h:m m:ss:xxx yy CR,LF	Display of status. Time and tape deck status yy acc. to list STATUS EQUATES x= msec and yy = byte "CODE" (escape with CTRL X or ESC)
STAT	STAT [-r ,] CR with -r = repeat	STATUS CR,LF	Display of status, according to table DISPLAY OF STATUS.
SON	SON [,:] CR	CR, LF	Synchronizer enabled
SOF	SOF [,:] CR	CR, LF	Synchronizer disabled
TDN	TDN [,] CR	CR, LF	Time code delay on
TDF	TDF [,] CR	CR, LF	Time code delay off
APE	APE [,] CR	CR, LF	Append mode enabled
APD	APD [,] CR	CR, LF	Append mode disabled
LWD	LWD [,] CR	CR, LF	Library wind disabled
LWE	LWE [,] CR	CR, LF	Library wind enabled
SMS < >	SMS <x.y> CR with 0.1<x.y<15.0	CR, LF	set max. wind speed
SWS < >	SWS <x.y> CR with 0.1<x.y<15.0	CR, LF	set library wind speed
MV?	MV? [,] CR	CR, LF	Move roller counter ? 4 byte, hex display

Display of Status

To escape from status display mode press ESC; to stop or start in repetitive mode press any other key

POSITION	BYTE	DESCRIPTION
1	1	Status of local keyboard 76543210 └──→ 0: enabled, 1: disabled
2	1	Status of remote keyboard 76543210 └──→ 0: enabled, 1: disabled
3	1	Status of master clock configuration 76543210 └──→ output sync 0: sector, 1: word └──→ ext. ref. input 0: balanced 1: unbalanced 000 ──→ ext. ref. video ebu 001 ──→ ext. ref. video ntsc bw 010 ──→ ext. ref. digital input (bal only) 011 ──→ ext. ref. synchronizer 100 ──→ not used 101 ──→ ext. ref. word sync. 110 ──→ ext. ref. video ntsc col └──→ input 0: extern, 1: intern
4	1	Status of sampling frequency 76543210 └──→ 0: not defined 1: 48 kHz 2: 44.1 kHz 3: 32 kHz 4: 44.056 kHz └──→ 1: lower sampling rate (LO) 2: higher sampling rate (HI)
5	1	Status of actual display 0: timer 1: watch or lap 2: time code 3: reference time
6	1	Status of safe/ready 76543210 (0: ready, 1: safe) └──→ channel 1 └──→ channel 2 └──→ aux 1 (TC) └──→ aux 2 (RT) └──→ aux 3 (ch2/aux) └──→ aux 4 (ch1/mix) └──→ master
7	1	Status of repro/input 76543210 (0: repro, 1: input) └──→ channel 1 └──→ channel 2 └──→ aux 1 (TC) └──→ aux 3 (AUX)
8	1	Status of actual tape type 0: tape A 1: tape B

POSITION	BYTE	DESCRIPTION
9	1	Status of fader 76543210 00→ fader A 01→ fader B 10→ fader C 11→ fader B → fader prepared → fader active
10	1	Status of autoinput 76543210 → autoinput A → autoinput B → 0: automute, 1: autoinput according bit 0 & 1
11	2	Status of toggle keys Base + 0 76543210 → autoedit 0: off, 1: on → automute 0: off, 1: on → rehearse 0: off, 1: on → not used → level display permanent 0: norm 1: input → varispeed 0: off, 1: on → ignore di c word 0: off, 1: on → channel control parallel 0: off 1: on Base + 1 76543210 → not used → high pas filter 0: off, 1: on → not used → play cue 0: analog 1: automatic → input 0: digital, 1: analog → not used → emphasis 0: off, 1: on → quality display 0: off, 1: on
12	4	Status of constant relative tape time [HEX]
13	1	Status of lifter 76543210 → 0: normal control from tape mpu 1: lifter disabled → 1: lifter enabled
14	1	Status of locator 00H : no locator 01H : locator 1 02H : locator 2 03H : locator 3 04H : locator 4 05H : locator 5 06H : last play / stop position 07H : last play / play position 08H : last play / record position 09H : reserved 0AH : set timer 0BH : set address 0CH : rollback / stop time 0DH : rollback / play time 0EH : rollback / record time 0FH : zero

POSITION	BYTE	DESCRIPTION
15	1	Status of varispeed display 76543210 00→ inch per second 01→ half tone 10→ % → indicator enhanced
16	1	Status of varispeed selection 00H : -12.5 % 7DH : 0 % > step = 0.1 % (01H) FAH : 12.5 % /
17	4	Status of error handling Base + 0 : error definition Base + 1 : error number Base + 2 : Base + 3 : > address of error definition

Status Equates

CODE	DESCRIPTION
01H	TAPE OUT NOT ACHIEVED
81H	TAPE OUT ACHIEVED
02H	STOP NOT ACHIEVED
82H	STOP ACHIEVED
03H	REWIND NOT ACHIEVED
83H	REWIND ACHIEVED
04H	FORWARD NOT ACHIEVED
84H	FORWARD ACHIEVED
05H	NOT USED
85H	NOT USED
06H	NOT USED
86H	NOT USED
07H	PLAY INTERNAL REFERENCE NOT ACHIEVED
87H	PLAY INTERNAL REFERENCE ACHIEVED
08H	NOT USED
88H	NOT USED
09H	RECORD NOT ACHIEVED
89H	RECORD ACHIEVED
0AH	NOT USED
8AH	NOT USED
0BH	EDIT NOT ACHIEVED
8BH	EDIT ACHIEVED
CODE	DESCRIPTION
40H	SHUTTLE BACKWARD NOT ACHIEVED
0C0H	SHUTTLE BACKWARD ACHIEVED
41H	SHUTTLE FORWARD NOT ACHIEVED
0C1H	SHUTTLE FORWARD ACHIEVED
42H	LOCATE WIND BACKWARD NOT ACHIEVED
0C2H	LOCATE WIND BACKWARD ACHIEVED
43H	LOCATE WIND FORWARD NOT ACHIEVED
0C3H	LOCATE WIND FORWARD ACHIEVED
07H	LOCATE PLAY BACKWARD NOT ACHIEVED (*)
07H	LOCATE PLAY BACKWARD ACHIEVED (*)
07H	LOCATE PLAY FORWARD NOT ACHIEVED (*)

CODE	DESCRIPTION
07H	LOCATE PLAY FORWARD ACHIEVED (*)
46H	CUEING BACKWARD NOT ACHIEVED
0C6H	CUEING BACKWARD ACHIEVED
47H	CUEING FORWARD NOT ACHIEVED
0C7H	CUEING FORWARD ACHIEVED
48H	NOT USED
0C8H	NOT USED
49H	NOT USED
0C9H	NOT USED
4AH	NOT USED
0CAH	NOT USED
4BH	NOT USED
0CBH	NOT USED
CODE	DESCRIPTION
59H	TAPE DUMP NOT ACHIEVED
0D9H	TAPE DUMP ACHIEVED
5AH	CUT WITH DISTANCE NOT ACHIEVED
0DAH	CUT WITH DISTANCE ACHIEVED
0DDH	BURN-IN TEST ACHIEVED

(*) Composite command/status message. The last transmitted command is indicated. 07h (play internal reference) is indicated after termination of locate play backward or forward.

Examples:

>FWD =	fast forward
>STP =	stop
>LOC_-01_43_00_800 =	locate to address - 1.43.00.800
>SAF_3/ =	time code channel SAFE (recording inhibited)
>GA?_1_0A* =	request for analog output gain value, channel 1: answer of the recorder e.g. A9 HEX
>SAP_1_O_8.3* =	set analog output level channel 1 to 8.3 dBV.7; the old value will be overwritten
>DU_24C_267 =	All tape tension parameters are displayed on the terminal in hexadecimal format, e.g.

```
     0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
0240 xx xx xx xx xx xx xx xx xx xx xx xx 00 83 87 82  ................
0250 00 00 E5 EC 00 00 00 00 01 2D 82 00 00 00 00 00  ...........-....
0260 3C F0 80 00 09 90 00 00 xx xx xx xx xx xx xx xx  <...............
0270 .. .. .. .. .. ..
.... .. ..
....
```

The address of a parameter can be computed by adding an offset which is tabulated in a separate list to the start address.
For start address see section MASTER MONITOR, command "LABEL" in volume III of the D820X manual.
For offset address see section MASTER MONITOR, command "PARAMETER" in volume III of the D820X manual.

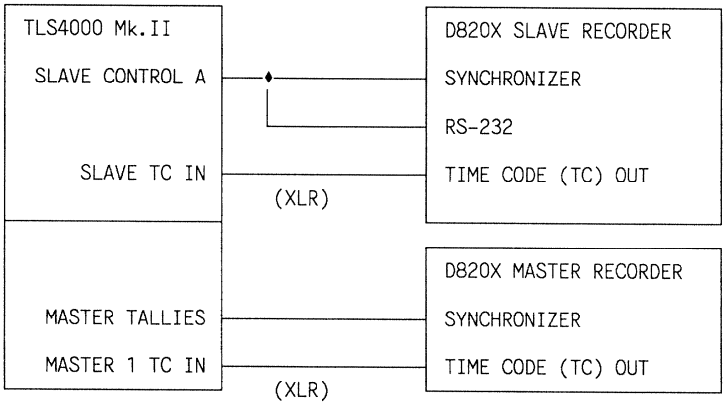
2.10.6 Operation of the ES Interface

To be defined.

2.11
Operation with Synchronizer

Connection and Operation

1. SLAVE Recorder(S) Connect the synchronizer parallel port (DSub25 connector) and - if necessary - the serial port (DSub9) to the synchronizer. For the latter, option 1.810.751 Serial Remote Controller (ASCII or binary protocol) must be fitted to the recorder (see par. 2.4.1.7, remote control connector and par. 2.10.3A ff.). Studer TLS4000 Mk. II synchronizers derive only move pulse information and the capstan reference signal from the parallel port. Most functions can be performed with these interconnections. The synchronizer automatically initializes with SYNCHRONIZER ON and "no echo" mode, otherwise press key SYNCHRONIZER ON (function 023 in the audio keys/mode menu) and/or disable echo mode (alignment deck menu, ASCII RS-232 mode). Establish a proper synchronizing source for the recorder to lock upon (internal or external sync). Refer to par. 2.6, key SYNCHRONIZER, for information on behavior and set-up of the recorder. Note that the synchronizer itself is also a synchronizing source for the recorder! Additionally connect time code output to the slave TC input of the synchronizer (see figure below).



Interconnection of TLS4000 Mk.II synchronizer with D820X master and slave recorders

Devices and cables:

Studer TLS4000 Mk.II Synchronizer		69.088.12301
with software	(master)	1.812.900.22 up
	(signal)	1.812.901.22 up
	(capstan)	1.812.902.21 up
Interface D820X		1.812.436.20 up
with software		1.812.969.20 up
Interface cable Mk.II, 1.5m		1.023.752.00
Interface cable Mk.II, 5m		1.023.758.00
Interface cable Master Tallies		n.a. (see table below)

When a synchronizer is connected, the slave recorder is under its command. During STOP, for instance, signal /SR-VRSPD/ is logical low (chase phase). All internal and external sync sources - except synchronizer - are disabled. Since digital input (DI) is also a sync source, it will also be disabled during STOP. In order to establish normal operation, the "lock" mode of the synchronizer has to be disabled.
When a recorder operates with external clock in PLAY or RECORD mode, interruption of this condition by the synchronizer is possible. Activating "store offset" compensates time code address discontinuities. The "on air" function available on Studer TLS4000 Mk.II synchronizers is the most reliable function to freeze all operational modes of the slave recorder(s).

The D820X can lock to synchronizing sources over a wide frequency range:
CAPSTAN SPEED CONTROL OF SIGNAL /SR-REFEXT/: 6...13.5 kHz
RANGE OF VALID DIGITALAUDIO FOR /SR-REFEXT/: 6...11.3 kHz

Caution: out-of-range signals may cause permanent muting conditions! Power-down may be necessary to establish normal operation.

Synchronizer operation in varispeed mode: when the master has a speed offset (which is identical to a sampling frequency offset) the slave will be immediately out-of-lock after completion of the chase phase due to the speed offset between the recorders. It attempts to re-synchronize ad infinitum.

Muting modes with TLS4000 Mk.II:
DIL-switch 2 on Synchronizer Interface board OFF: mute enabled
DIL-switch 2 on Synchronizer Interface board ON : all mute commands ignored
DIL-switch 4 on Synchronizer Interface board OFF: mute until lock is established
DIL-switch 4 on Synchronizer Interface board ON : demute during chase and lock phase (*)

(*) there is a short mute between chase and lock phase, its duration depends on the synchronizing source in lock mode (see par. 1.6, technical specifications, clock in- and outputs).

2. MASTER Recorder For improved tape deck performance of the slave(s) (reaction time to STOP, PLAY, RECORD and WIND mode, when time code readout is out-of- range) connect the synchronizer parallel port (DSub25) of the master recorder to the master tallies connector of a TLS4000 Mk.II synchronizer.

D820X External Synchronizer Connector			MASTER TALLIES
Pin	Signal name	Description	Pin Number
01	+0.0	ground	01
07	OR-MVCLK *	output for TAPE MOVE CLOCK signal (512 pulses/second, duty cycle=50% for 48 kHz sampling frequency)	03
08	KEY	coding	
09	BR-REC *	lamp RECORD achieved	08
10	OR-MVDIR *	output for signal TAPE MOVE DIRECTION (rewind=LOW, forward=HIGH)	09
14	+0.0	ground	05
15	BR-PLAY *	lamp PLAY achieved	04
16	BR-STOP *	lamp STOP achieved	02
24	KEY	coding	

* Open collector output, active LOW. No internal pull-up resistor, max. HIGH level = 30 V. Sink current 200 mA max., internal current limiting resistor 22 Ohm.

\+ Switch input, LOW level activates command. Internal pull-up resistor 4.7 kOhm connected to +24 V, max. HIGH input level = 30 V. Logic levels: LOW: 0 V to 4 V; HIGH: 7.5 V to 30 V.

Note that the synchronizer is set to accept a move clock signal with 512 pulses (TLS4000 Mk.II: User Keys), otherwise over- or underreaction results.
For detailed operating intructions of the synchronizer itself refer to the corresponding manual.

2.12
Optional Software Support

Description of D820X optional floppy disk for servicing and diagnose

Connecting a personal computer to the D820X:
an uncrossed interconnection from the "test" connector of the D820X (DSub25) to the personal computer should be established. Format: RS-232.

Conditions to start the monitor program:
the D820X should be in power-up mode and the initialization must be completed. When the personal computer is used in terminal mode, the program VTERM (on IBM computers) must be called and terminated with "CTRL" and "BREAK".

Conditions during use of the monitor program:
the D820X may not be switched off during use of the monitor program. When the D820X has to be switched off proceede as follows:

1. go back to the main menu: press M
2. escape from the program : press E

Now disk drive level is reached again and the prompt "A: >" appears, indicating access to drive A.

Start of the program:

- Choose the appropriate storage medium: i.e. if the file is on a floppy disk inserted in drive A, press "A:" and "RETURN".
- Call the monitor program with "BWRUN" or "MONRUN" respectively, followed by "RETURN". On the screen, the messages

  echo off
  -wait-
  system ready

  appear ("system not ready" appears if there has been a mistake).

After that the main menu appears with the title

D820X: SERVICING AND DIAGNOSE

The menu itsef is menu-driven.

Remarks: "DWRUN" is the monitor program for black-and-white monitors (standard configuration for IBM-XT); "MONRUN" is the monitor program for color monitors (standard configuration for IBM-AT).

If the above mentioned sequence has not been followed, a so called 'warm-start' of the computer may be necessary: press "CTRL" plus "ALT" plus "DEL" simultaneously (valid for IBM computers), or consult the manual of the personal computer.

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3 Technical Description

3.1 Board Distribution

3.2 General Description

3.2.1 General Information

3.2.1.1

The Control BUS

The PCM control bus is a relatively high speed serial bus system with a clock rate of approx. 1.25 MHz, providing communication of control information between digital audio, panel, cage and PDM electronics. The bus is controlled by the system controller (Syscon 1.861.763), see par. 2.8 below.

The hierarchical structure of processors:
Level 1: master processor
Level 2: Syscon, tape deck processor, capstan processor, RS-232 bus processor, ES-bus processor, int. synchronizer, etc.
Level 3: display processor, audio signal processors, etc.

Level 1 and 2 processors communicate via an SSDA protocol (in par. 3.2.4.1 a short description of this protocol is given), while the Syscon communicates via control bus (Sysbus) with its slave processors and hardware. This type of communication is defined in the chapter "communication between syscon and hardware" in par. 4, vol. III of the D820X manuals. The higher level processor is always the master of its bus, so that no bus arbitration scheme is required (the master polls its slaves).

Specifications of the sysbus

```
Clock rate  : approx. 1.25 MHz
Lines       : - clock,   SYSCLK
              - address, SYSADR (separates data from addresses)
              - data,    SYSDAT all balanced according to RS-422, serial
```

Bus length : 10m max.
Terminations: at the analog output end of the BACKPANEL BOX (1.861.885), on the PCB Backpanel Cage (1.861.895), at the output of the Display Interface (1.861.817) in the Display Processor (1.861.742). The CCP Transceiver (1.861.744) contains jumper connectors which should be inserted when no display panel is connected to the channel control panel. No other termination resistors are allowed and necessary.

Each module on the bus is addressed with a unique binary address, followed by data byte(s). Data-transmission is bidirectional, indicated by bit I (see below).

Formatting of Syscon addresses:
(normal format)

```
         AAAA SSSI DDDDDDDD
         **** ***
A = device address, MSB first
S = subdevice address
I = low, if tx; high, if rx (related to hardware)
D = Data bits, MSB first
* = Syscon address
```

A special format used to transmit digital gains and all Syscon addresses can be found in the list "communication between syscon and hardware" in vol. III, chapter 4 of the D820X manuals.

The following boards contain Syscon receiver and/or transmitter modules: Detector (located in cage), Analog Input, Analog Output, Gains Control (DAPRO), Codec Control

(Codec), Timing + Test, RT/TC Codec, PDM Control (located in rack), Display Panel (may be located remotely), Channel Control Panel, Monitor Panel. Syscon modules located in panels or in remotes are buffered in the Display Interface board 1.861.817.
A selection of bus modules has been standardized for the D820X: 2 byte receiver, 8 byte receiver, 2 byte receiver/transmitter and 8 byte transmitter.

Important note: **disconnect power bevore removing boards containing syscon modules!** Its drivers are very sensitive to surges at their outputs.

3.2.1.2

Servo Control

Several modes are possible: in RECORD the servo is controlled directly by a crystal reference (in nominal speed), or from a frequency derived from the varispeed-PLL (in varispeed mode), or from sector sync (RT SYNC mode) in track sequential recording. In REPRODUCE the servo is controlled either from the block syncs (at least 5 tracks must contain reliable data) or from sector syncs in RT SYNC mode. The latter is required for playback of a track sequential recording. Servo control from the data tracks (block syncs) is preferred over control from the reference time track due to the higher resolution (one sector contains four blocks) with shorter locking time in case of sector discontinuities (tape-cuts, etc.) and due to a higher immunity to dropouts and trackloss (eight data tracks can be analyzed compared to one reference time track). Servo control from data tracks is derived on the Transformatter board. The RT/TC Codec board processes reference time data. The signal T-REFINT is generated on the Transformatter board out of one of three sources (master clock, block syncs or sector syncs) (refer to par. 3.2.2.4) and is fed to the Capstan Interface board via Master Syscon IF board, both located in assembly 11.

In the so called chase-lock phase, when the recorder is controlled from a synchronizer, a frequency proportional to the external synchronizer reference (signal T-REFEXT) controls the capstan servo. The external signal is fed via Parallel Remote Interface to the Master Syscon IF and then to the Timing + Test board on which the entire timing changes proportionally to the external frequency and with it the timing of the IC on the Transformatter board which generates the signal T-REFINT as described above. No servo loop via tape is established in this mode.

3.2.1.3

Alignment

Alignment is required at two different places:
a) on tape
b) at the outputs of the recorder.

a) Alignment on tape

Precise alignment on tape is needed in order to reach tape interchangeability. The sector edges of the reference track and the edges of blocks with addresses 00 must be in geometrical alignment with a tolerance of ± 0.5 block.
Cue and time code signals are written at the theoretical center of the data, which have been spread over a distance of 323 blocks.
With in-line write heads, the cue and time code signals therefore have to be delayed by 161.5 blocks plus additional encoding delays which occur in the modulator, encoder, etc. In the D820X these delays are implemented on the Cue/PQ Delay board 1.861.816 for cue signals (the auxiliary track 3 is not delayed when used as a data track), and on the RT/TC Codec 1.861.761 for time code signals. Both delays are clocked by the system clock and maintain their proper values without adjustment when the sampling rate is changed.

b) Alignment at the outputs

Reference time is aligned with data in the D820X, which means that reference time has been time base corrected. Time code is aligned with data but not time base corrected. The transitions of time code will jitter relative to data or reference time due to the wow

and flutter values of the recorder. It is necessary to set the appropriate frame rate in the menu (functions 401...405).
The cue outputs are neither delayed nor corrected. There is an audible time difference when the analog outputs of the main channels are monitored on loudspeakers and compared to the cue outputs.
There is no time difference between the two main channels.
Phase relationship of wordsync is maintained from in- to output in analog or digital input mode and when synchronized via wordsync. The trailling edge of wordsync is located in middle of channel A MSB.

3.2.1.4 **Power Supply Distribution, PCM Part**

The power supply box generates 3 voltages partially required in the box itself: +5 VDC, ±20 VDC and +20 VDC, designated +20PC. The latter is fed via box-rack interconnection to the Backpanel Rack, together with its ground (+0V-). These 20 V are distributed to the Delta-Molex Interconnection board, the Channel Control Panel and the Display Panel. All these assemblies utilize on-board switching regulators to derive +5 VDC from +20PC. The Delta-Molex Interconnection board produces +5.6 VDC for the head electronics in the cage. +5.6 VDC for the Monitor Panel is derived from the switching regulator 1.861.790, located in assembly 11. Both 15 V supplies (± 15 VDC) for the Monitor Panel and the cage electronics are also derived from the switching stabilizer 1.861.790. These voltages are further regulated in the cage to 10 VDC on the Playback Amplifier 1.861.808 for the noise-sensitive read electronics.

3.2.2 PCM-BOX: Description of Boards and Assemblies

3.2.2.1 **Analog Input 1.861.752/1.861.753**

Purpose: Conversion of signals, applied to the analog line input, to serial data; limiting signals above the Nyquist frequency.

Features:
- self-contained boards, accepting balanced/unbalanced line level signals at input and containing digital circuitry necessary for 16 bit serial data output.
- 16 bit performance.
- two stage converter design (2*12 bits) with 8 bits overlap for increased stability (gain and offset errors).
- successive approximation converters.
- anti-aliasing filter 9th order, together with 4th order phase compensation, 24kHz bandwidth, very low ripple.
- input for dither signal.
- DC response possible.
- software controlled gain adjustment.

The Functional description of each circuitr block is given below.

3.2.2.1.1 **Input Stages**

The board 1.861.752 is equippped with an input stage without transformer, which converts a balanced floating input signal (or an unbalanced) to an asymmetrical output signal. On the board 1.861.753 the same operation is performed with a transformer, permitting galvanic separation between the preceeding stage and the D820X input. The input without transformer is proteced against excessive DC input voltages and the CMRR can be trimmed to a maximum. On the input stage with transformer the secondary resistance of the transformer is corrected by applying positive input impedance, resulting in excellent distortion behavior. Both input stages are designed to suppress HF signals above the audio band.

3.2.2.1.2 **Gain Control**

An MDAC controls input line level in the range 0...20dBV.7. Each board contains a 2 byte Sysbus receiver for this purpose, which allows adjustments to be made from the LCD display of the recorder, from the display panel or from remote locations. Factory adjusted level trimming (fine) is made with a potentiometer on the board.

3.2.2.1.3 **Emphasis**

This circuit accentuates high frequencies by about 10db with time constants 50 and 15 µsec. in "emphasis on" mode. Signal /FLEM/ is input from the Gains Control board 1.861.853.

3.2.2.1.4 **Phase Correction**

The preceding filter is 4th order phase corrected up to 20kHz with two second order allpass sections.

3.2.2.1.5 **Filter**

The anti-aliasing filter is a 9th order elliptic lowpass, implemented with frequency dependent negative resistance (FDNR) stages, in order to obtain a wide dynamic range and low sensitivity to low frequency stray fields. The filter is designed for very low ripple up to 24 kHz and its stopband attenuation is greater than 60dB. The circuit and the level diagram were carefully designed for low THD+N values, not exceeding 0.0025% in the passband for input levels ≤10 dBV.7. Both the anti-aliasing filter and the phase correction may be bypassed by means of a jumper wire at the output of the filter. Note that in this case the gain of the track & hold stage should be increased by 4.6 dB.

3.2.2.1.6 **AC-Coupling**

Normally, the board contains a capacitor to limit the low frequency response. The cut-off frequency is around 2 Hz. It is possible to obtain a response down to DC if the input stage without transformer is used and the capacitor is replaced by a wire. Then, however, the offset produced by the ADC will cause a reduction in usable dynamic range.

3.2.2.1.7 **Dithering**

An inverting amplifier with 40 dB attenuation is connected to the summing point of the track & hold. It accepts any kind of analog dithering noise. Maximum signal level at this insertion point is 5 Vp (13.2 dBV.7).

3.2.2.1.8 **Track & Hold**

The circuit basically comprises of an inverting amplifier stage with the switch current-driven on virtual earth. The hold capacitor is in the feedback path of the fast track & hold amplifier, with an additional capacitor of equal value for balancing-out charges during switching and to provide unity gain stability. A second amplifier serves essentially as charging amplifier. Minimum sample time for specified performance is approx. 3 µsec. Note that severe constraints are applied to the timing jitter of the sample signal.

3.2.2.1.9 **Gain 1st and 2nd Conversion**

A gain of 2/5 during the first conversion enables an optimal level diagram and an acceptable resistance level during second conversion, where a gain of 32/5 is applied for 8 bits overlap of the two conversions. With the two factory adjusted potentiometers, the gains for first and second conversion can be adjusted. The goal is to obtain minimum THD+N.

3.2.2.1.10 **ADC**

A two-stage succesive approximation design with residual extension is implemented with a comparator, a 12 bit DAC and PAL/GAL-shift registers (MSAR-A, MSAR-AB, MSAR-B). During the first conversion a 16 bit DAC applies a mid-level DC signal to the summing junction in front of the gain switching amplifier. The latched 12 bit data from the first conversion is then subtracted from the input and amplified. A second ADC

cycle provides fine conversion (again 12 bit). Parallel data from both conversions are stored temporarily in a 64 bit RAM and added in PAL/GAL ADDRAM after parallel/serial conversion in MMX and and shifting right by 4 bits to compensate for the analog gain in PAL/GAL INTER. The same PLD also provides sign extend of the 4 MSB's of the second conversion. This configuration ensures great tolerance against gain and offset errors (8 bit overlap). The outputs of RAM (coarse and fine conversions of both channels) are latched bevore they are cycled back to PAL/GAL INTER. Serial output data and valid signal are in RS-422 format. Timing signals START and CLK are received differentially. An additional output signal (ADCCLIP1/2) indicates overload conditions and may be used for an external clipping circuit and overload display. With a potentiometer (factory adjusted) the offset voltage is trimmed to obtain maximum voltage swing.

3.2.2.1.11 **Feedback Correction**

Since the performance of the conversion can only be as good as its reference, the 5 MSB's of the feedback DAC have been corrected. Therefore each 16 bit DAC is assorted with a correction PROM. An 8 bit correction DAC is used in a feedforward configuration with the main DAC. Optimal matching of output currents of the main and the correction DAC is achieved by a factory adjusted trimm-potentiometer. In order to obtain full performance of the system, the customer is advised not to change main DAC's individually, but to replace both main DAC and correction PROM at the same time by a matched set.

3.2.2.1.12 **Timing**

The PLD MASTER produces addresses for a 2k PROM, organized in 256w by 8 bits, which in turn generates addresses for a RAM, the SAR registers and the parallel/serial registers, and for the PLD FLGEN, which generates gain setting and sampling signals (among others).

3.2.2.2 **Data Processor (DAPRO)**

The data processor (DAPRO) consists of the boards Gains Control 1.861.853, Dapro Interface 1.861.854, Data Processor 1.861.855 and Coefficient Generator 1.861.856. Their major operations are:

- to perform data concealment (interpolation, hold and mute) by means of a crossfiltering circuit
- splice processing
- provide interfacing to the selected in- or outputs (analog or digital, according to AES/EBU format)
- provide interfacing to the Codec boards
- a highpass function to remove DC content of the selected input source
- digital gains adjustment
- punch-in and -out level fades (not used)
- in the twin implementation: error correction by utilizing the "backup" track
- feeding clipping and level information to the System Controller to be displayed on the display panel
- performing a holding function of the analog input signal (after it has been digitized) as long as clipping is indicated by the Analog Input board.

.v.:::3.2.2.2.1 **Gains Control 1.861.853**

Contains:

- an 8 byte receiver connected to the sysbus: 3 bytes carry different "toggle" functions, like input selection between analog and digital (ADCAES) or sampling frequency selection (SAMP48) among others, and 5 bit are occupied by punch-crossfade values (CROSSTIM), used during initialization. Two bytes carry DAPRO gain addresses and values (DPGNADRD and DPDIGGN) for direct update of digital gains, independent for each channel.
- an 8 byte sysbus-transmitter, 3 bytes are used: one byte for clipping information (DPCLIPP) and two bytes for bargraph and peak level indication (DPLVLCH1/2), both are displayed on the display panel. Additional circuitry compresses 13 bit linear

PCM data from bus 5 for a 50 dB lin/log bargraph-scale and retains the last peak value until the register is cleared by the system controller. The (digital) clipping information is derived on the Data Processor board.

3.2.2.2.2 **A DI-PLL 1.861.730**

Together with the sync and edge detector and the AES/EBU receiver it forms a self-contained unit with the function to read the content of the control word without prior knowledge of the sampling frequency. At the reference input of the PLL one of three currently used sampling frequencies (fs) is applied (44.056, 44.1 or 48 kHz). The feedback counter, connected to the other input of the PLL divides the output frequency by 256, which defines the output frequency to be 256 * fs, two times the cellclock needed to read digital input data.
The input signals are applied to a phase detector (IC6), which produces a difference signal proportional to the input phase. This signal is then fed to an operational amplifier in inverting configuration (IC4) which builds a second order loop filter. Its time constants are choosen for short capture time and best smoothing behavior (contradictory requirements). An offset voltage is applied to the positive input of the amplifier, which is needed by the following voltage controlled oscillator (VCO) IC1. Between these two is a passive filter first order (R1, C1) a variable capacitance diode (varicap) D1 and a tank circuit formed by L1. The selfinductance of L1 has been chosen so that the output frequency is limited to the operational range of LS-TTL circuits when the input frequency is disconnected (uppermost frequency in this mode: typ. 21 MHz). The output of IC1 is connected to a fast comparator (IC5) which serves as buffer and drives the following logic circuits with their associated wiring.
The rest of the board space contains voltage regulators and bypass capacitors because even for this application, a fairly high jitter performance of the output waveform is required. More stringend requirements are placed on DUAL PLL 1.861.725 which is described in par. 3.2.2.8.2 below.

3.2.2.2.2 **Dapro Interface 1.861.854**

Contains:

- serial inputs from the Analog Input board or from the AES/EBU receiver (digital input), which may be routed to the parallel processor bus via DAPRO main input registers which are under software control. The input is selected via PLD, which also generates several required control signals. For the AES/EBU input a data buffer is implemented to synchronize source and sink without word slip.
- the following serial outputs are connected to the parallel processor output bus under software control:
- d/a1 analog output (repro/input)
- aes/ebu1 digital output (repro/input)
- pdm cue output (input mode)
- enc encoder output (input mode)
- registers, connecting the parallel input bus 3 to the parallel output bus 5 for testing purposes.

3.2.2.2.3 **Data Processor 1.861.855**

Contains:

- a standard program for i/o timing and basic gain multiplication.
- a hardware/software structure allowing in a first sequence a different routing in cases of gain value changes, muting and repro/input selection; and in a second sequence a different routing in cases of error concealment and splice handling.
  A program sequencer on this board permits all functions to be controlled by software.
- routing information, provided by the different flag registers, is fed to the program segment address selector PROM's. When the program step counter is loaded and starts counting, the PROM's generating the program code control the arithmetic units and the i/o devices and prepare the next program segment address via the program segment address selector PROM's.
- additional circuitry for the high pass filter, the clipping circuitry and parts of the arithmetic unit.

3.2.2.2.4 **Coefficient Generator 1.861.856**

Contains:
- several of the PROM's generating program code.
- the circular address generator and PROM (3), which handles the resulting address, depending on the circular address and the program segment address.
- the increment PROM's (1) for muting, splice and other constants; the increment PROM's (2) for different punches.

3.2.2.3 **Codec**

In the channel encoder part, digital data is protected against channel errors by adding parity bits. Because the channel mainly displays a burstlike error behavior, interleaving is used to spread the errors out over a longer periode of time (scrambling data). This is preceded by a matricing operation before the encoder to distribute the samples on the tape as required by DASH-Twin recording. The decoder re-orders the data and separates redundant information. It also checks the parity sums and corrects erroneous data, as long as the error pattern is within its correction capabilities. It also detects interleave errors which indicate splices and feeds the necessary flags for splice handling and error concealment to the data processor (DAPRO). The operations carried out in the encoder delay data by 4 blocks.

To summarize: the functions of Codec (Control and Memory board) are
- matricing (track sequencing)
- d, D, odd-even interleaving/deinterleaving (different delays)
- P and Q parity computation during encoding and decoding
- detection and correction of interleave errors and overwrite dropouts
- detection of splice, concealment and mute conditions
- generation of splice, sample and mute flags for DAPRO
- generation of signal quality information for display

3.2.2.3.1 **Codec Control 1.861.857**

Codec Control generates addresses and microcode for an 8 track time division multiplex. The microcode incorporates program segments for track encoding and decoding and a program for channel/track matricing.
A muting circuit detects tape errors exceeding the error correction capabilities of Codec and marks data for later processing in the DAPRO boards. Codec Copntrol also generates a control signal for the crossfilter section in DAPRO, if long dropouts occur on tape.
A splicing circuit detects general data discontinuities and generates protection (error flags) when interleaved data is detected and produces a control signal for the crossfilter (on the DAPRO boards) in case of tape-cut.
A 2-byte transmitter/receiver communicates with the System Controller. The transmitter sends one byte of decoder error state information which can be read-out either as signal quality or as blockerror rate. The transmitter sends one byte of decoder error state information which can be read-out either as signal quality or as blockerror rate. The receiver may be fed with one byte of testing information, simulating most tape errors. Processing electronics can be tested with these simulated errors.

3.2.2.3.2 **Codec Memory 1.861.858**

The parity arithmetic which communicates via 16 bit data bus is interfaced serially with the DAPRO boards (LSB first) and with the Transformatter (MSB first). The interface timing and hardware supports electronics-to-electronics loops either before or after Codec (loops 3 and 4).
For the DASH-Twin implementation, a latch connected to the 16 bit data bus generates twin tracks.
The use of high speed RAM's permit the implementation of a highly multiplexed organisation.
The length of the Codec program (288 steps per track, organized 16 bits by 18 words) permits P-Q encoding and a sophisticated Q1-P1-Q2-P2 decoding (patent pending).

3.2.2.4 **Transformatter 1.861.859**

The Transformatter consists of the following functional sections, which are described below:

3.2.2.4.1 **Reference Address Counter**

The counter runs synchronous to the RA-counter (reference address counter) in the Codec and generates bit-, word- and blockaddresses of serial data for internal processing in the Transformatter.

3.2.2.4.2 **Formatter**

The formatter receives serial data from the Codec and supplements them with a sync word (with flags and block number) and the CRC word. Serial data is converted from a track-serial to a track-parallel format with the formatter RAM. A delay of 1 block arises from this operation.

3.2.2.4.3 **Modulator**

Serial data from the formatter are converted to a modulation scheme, called HDM-1, which is essentially a bit mapping operation. This ensures that

- the frequency spectrum after the read head has low power at low frequencies
- the bit clock frequency can be regenerated from the signal delivered by the read head
- intersymbol interference caused by the tape is kept low, by imposing a lower limit on the length of a sequence of ones or zeros. HDM-1 ensures a minimum run length of 3 and a maximum of 9.

Conversion from serial NRZ-data to HDM-1 data is done in time multiplex for all 8 channels.

3.2.2.4.4 **Data Synchronizer**

Data which is read from tape for each track individually will not arrive at a constant rate. It is fluctuating in time referred to a quartz reference, due to wow and flutter and other mechanical deficiencies. A buffer register (time base corrector or data synchronizer) eliminates these effects. The data synchronizer works in bit serial form and feeds the Codec with data in track serial form.

3.2.2.4.5 **Cyclic Redundancy Check**

Each block of read data is checked for CRC errors and, together with an appropriate flag, sent to the Codec for further processing.

3.2.2.4.6 **Actual Block Address Generator**

The actual block address is calculated from the block address encountered at the output of the data buffer and from the filling state of the buffer (for RT alignment). The addresses used for calculation are CRC checked. To compensate for deviations between the tracks a maximum likelihood detection is employed. If there are not enough addresses available, the result is extrapolated.

3.2.2.4.7 **Tape Cut Detection**

A signal ISPLDET is produced on the board, which is an OR-ed combination of two signals: one checks syncs from the data for their time coincidence (arrival in time), the other checks block numbers. When block numbering is continous, no splice signal is generated by this circuit.

3.2.2.4.8

Tape Speed Control

The circuit generates a square wave signal (TTL-level) for the tape servo control (T-REFINT) with frequencies

- 10.01739 kHz during write at 48 kHz (15.0 ips), or
- 9.2034782 kHz during write at 44.1 kHz (13.78125 ips), or
- 9.194284 kHz during write at 44.1/1.001 kHz (13.767483 ips), or
- 10.01739 kHz during write at 32 kHz (10.0 ips) with deviations of 2/230 from the above mentioned nominal tape speeds
- (-) 2/230 * fnom [Hz] during read (slow), or
- (+) 2/230 * fnom [Hz] during read (fast).

Slow/fast is controlled by the filling state of the data buffer or may be controlled externally by the RT/TC Codec, in RT SYNC mode.
Servo control may be derived from data when the incoming sync patterns of at least 5 tracks are available, or by means of the reference track. Servo control from the reference track is mandatory in channel sequential recording (for alignment on tape) or playback.

3.2.2.4.9

Testaids

A data generator may be activated externally. It produces a constant pattern in the formatter (16 bits high and 16 bits low successively). The CRC and sync words will be generated accordingly.
Via testloop 2 the formatted data can be connected directly to the input of the data synchronizer. It allows complete testing of the Transformatter with the exception of the modulator.
The detected CRC errors are displayed for all tracks at the same time and individually by 9 led's. CRC-errors, indicated by a transition, are also fed to an output, for convenient access.

```
TOP LED    * TRK0 / TRACK NO. 3 / DIGITAL 1 / 1A
           * TRK1 / TRACK NO. 4 / DIGITAL 2 / 2A
           * TRK2 / TRACK NO. 5 / DIGITAL 3 / 1A'
           * TRK3 / TRACK NO. 6 / DIGITAL 4 / 2A'
           * TRK4 / TRACK NO. 7 / DIGITAL 5 / 1B
           * TRK5 / TRACK NO. 8 / DIGITAL 6 / 2B
           * TRK6 / TRACK NO. 9 / DIGITAL 7 / 1B'
BOTTOM LED* TRK7 / TRACK NO.10 / DIGITAL 8 / 2B'
EXAMPLE: 2A': 2 denotes digitalaudio channel
              A track designator (A, B in M and twin formats)
              ' denotes backup track
```

3.2.2.5

Adaptive Run Processor 1.861.760

3.2.2.5.1

Purpose and Benefits

The Run Processor represents a data equalizer in digital form. A run is the time interval T between two consecutive differentiated pulses. The Run Processor corrects (equalizes) the main parts of which intersymbol interference in a tape recorder is composed:

- peak shift
- amplitude and phase deviations caused by the channel (tape)
- demagnetizing effects caused from neighbouring transitions, an effect most pronounced at short wavelengths.

The benefits from implementing the equalizer in digital form are:

- the actual run not only is computed from its history but also from its future
- there is no need for a PLL for clock extraction
- the same circuit is multiplexed for several tracks, saving space
- a detector, which adapts automatically to the tape speed may be implemented more easily
- no adjustments are needed
- equalization for several brands of tape may be software controlled
- it can be extended to higher order structures for even more reliability

- demodulation and sync detection is more easily implemented if the origin is already a run.

The priciple and implementation of the Run Processor is protected by several patents.

3.2.2.5.2 **Implementation**

Seven possible runs (from 3 to 9T) are written on the tape in random order, where 2T is the inverse of the data rate DR, DR=576kbit/sec.), read off tape for one track. Incoming data from the playback head in track serial form is converted to a run format. For this, the peak to peak distances from read pulses are counted. In an adaptive feedback circuit runs, quantized to 7 bits, are recognized to originate from one of seven possible written runs (3 bits of resolution), by means of a look-up table, fed with past, present and future runs as addresses. In a third part, demodulation is performed in time multiplex, as well as sync detection. A FIFO is included to separate consecutive runs. Demodulated data and sync are fed to the data synchronizer section of the Transformatter.

```
LED ARRAY FOR DISPLAY OF DANGEROUS RUNS
TOP LED    * RUN 9
           * RUN 8
           * RUN 7
           * RUN 6
           * RUN 5
           * RUN 4
BOTTOM LED* RUN 3
```

These LED's display the occurence of "dangerous runs", i.e. runs that do not exhibit a safe margin to adjacent runs and warn from induced noise into the heads or head electronics when the LED's are flickering in stop or wind mode. The LED's should be stable, otherwise too much noise is picked up by the heads or the head electronics which will degrade the CRC error rate. It may be necessary to remove terminals, personal computers, or other RFI generating devices located near to the headblock.

3.2.2.6 **RT/TC Codec 1.861.761**

3.2.2.6.1 **RT Eencoder**

The RT coder generates data for the reference time (RT) track:

```
 4 bit sync                )
16 bit flags               )  1 sector
28 bit reference address   )
16 bit CRC word            )
```

The flags and the reference address value are loaded via sysbus from the System Controller. The reference address value is incremented by one for each following sector. One sector corresponds in length and time to four blocks of digital audio data. The RT generator is synchronized from the Transformatter in order that each sector starts simultaneously with the first bit of a data block having address 00. The formatted RT data are bi-phase modulated and fed to the Write Amplifier.

3.2.2.6.2 **RT Decoder**

The RT decoder receives read data from the reference track, detects the sync word, demodulates the data and performs a cyclic redundancy check.
The received data is stored in an intermediate buffer memory and read out after some delay in the same format as received from the tape for external use (RT out). The delay is according to the momentary filling state of the data buffer memory (dasy) on the Transformatter. Due to this, data and reference time is aligned at the output of the data buffer memory.
Some of the read RT data (flags and reference address value) can be accessed by the System Controller any time. At the start of such a request cycle, the content of the last completely read RT sector plus the result of the CRC is transmitted.

When a correct CRC word has been read, a synchronizing pulse is fed to the Transformatter and used there to control tape speed in RT SYNC mode.

3.2.2.6.3 **Indicators**

(from top to bottom)

* CRC ERROR (of read rt data)

* DATA/RT SYNC MODE (illuminated in DATA SYNC mode)
* DASY FILLING STATE (red led, +1 BLOCK)
* DASY FILLING STATE (red led, +1/2 BLOCK)
* DASY FILLING STATE (green led, nominal value)
* DASY FILLING STATE (red led, -1/2 BLOCK)
* DASY FILLING STATE (red led, -1 BLOCK)

3.2.2.6.4 **Test Aids RT Codec**

The coded RT data is fed to the input of the RT decoder in EELOOP 3 and is visible on the LED TIME-display (switch to RT display, indicated with a leading index "r").

3.2.2.6.5 **TC Encoder**

Longitudinal time code (TC) in serial form and bi-phase modulated is applied to the TC IN connector (XLR-type) at the rear panel of the pcm box. It is received on the Connectorfield USA PCB 1.861.777, where it is galvanically de-coupled by a transformer stage and fed to the TC Analog IF II card (see next par.) 1.861.770, where an input buffer and a pulse shaper (comparator) is located. The ouput signal (EX) is applied to IC209 (PLD "SYN") which performs a reclocking operation of the asynchronous input signal to the timing of the recorder. Due to this operation, the original transitions of the TC signal may jitter by ±0.11 µsec. max. The PLD also divides clock 5 and controls the enable signal of counters IC 208 and IC 412 and the write signal of RAM IC 210. This RAM delays the input TC signal by 166.5 blocks in order to follow the alignment rules of the format. Since the RAM is clocked from the system timing, the delay is according to the selected sampling frequency. The TC signal is then subjected to discrete PDM modulation. For a logical low input signal a run of 3T is generated, for logical high periodes a run of 9T, when each input cell is divided into runs of 12T. The changes of the input cells do not necessarily correspond with the transitions of the above mentioned two states, therefore three merging runs may be introduced. This operation reduces additional jitter to ± 3 runs max., or ± 2.61 µsec. The modulation takes place in IC607 from which the signal is fed to the Write Amplifier via line driver IC 101. A parallel signal from IC 209 is connected to the demodulation path in INPUT or TEST mode.

3.2.2.6.6 **TC Decoder**

The signal from the read head is amplified on the Head Amplifier and the Playback Amplifier II 1.861.808 and differentially fed to the TC Analog IF II, where it is demodulated with a controlled lowpass filter if when has previously been subject to PDM modulation. If the tape has been conventionally recorded (bias) the signal is derived from a simple comparator stage. The signal TRO is the demodulated and TROM the non-demodulated signal. Both are input to IC211 which regenerates the signal. The four cascaded 4 bit counters IC309, 310, 311, 312 together with IC's 408 and 409 which are configured as 5 bit counters and are cascaded with the 4 bit counters generate the signal CEK which is the bi-phase clock signal (output of IC 408). It is fed to IC 212 where an out-of-range (OOR) and a direction signal (DIR) is produced.
The regenerated tc signal is written into RAM IC111 where it is delayed by 238.5 blocks (25 Hz frame rate) or 286 blocks (29.97 or 30 Hz frame rate). The correct frame rate is preselected by the user and fed via System Controller to IC510 and IC511 (syscon address decoders) from which the signal ABFRA for IC509 emerges. The correct frame rate adjustment ensures alignment of digitalaudio data with TC frames at the output of the recorder (wow and flutter not eliminated).

The delayed information can be accessed by to ways:

a) from the System Controller:
IC608 and IC410 generate the pointer for the read address, IC609 generates the enable and chip select signals, IC509 (configured as a shift register) transmits the bi-phase data via buffer IC110 to sysbus.

b) from the serial output:
IC611 and IC512 generate the pointer for the read address, the signal DTD is fed to IC212 from which it is output as signal TCEX to the TC Analog IF card.
IC411 and IC610 generate the pointers for the write address. The write enable signal for the RAM is produced in IC609. IC112 and 508 receive signals from the System Controller. Some of them (FRAMERA, MVARI and TAPETYPE) are fed to the Run Processor.

3.2.2.6.7 **Test Aids TC Codec**

An EE-loop can be formed by pressing key INPUT or selecting it via terminal or PC. The TIMER display must be set to time code (indicated with a leading "t").

3.2.2.6.8 **TC Analog IF II 1.861.770**

It consists of four sections:
a) the PDM demodulator, b) the sidechain for clock recovery, c) the input amplifier and c) the output amplifier.

The time code signal from the Playback Amplifier II 1.861.808 is received with a differential amplifier (IC12) and fed to both sidechain and demodulator. The demodulator comprises of a controlled lowpass filter (IC7) which is implemented in switched-capacitor configuration. This filter reconstructs the baseband content of the signal and removes the carrier. Its cutoff frequency is proportional to the tape speed, because its clock is derived from data. The clock frequency must be 50 times the cutoff frequency for this IC. It is followed by an active lowpass filter of second order which removes the switching transients from IC7. IC2 is a comparator with hysteresis and it shifts the input level (bipolar) to TTL-level for the successive logical circuits.
The sidechain starts with a comparator with adjustable hysteresis (IC11). Its output is used when a conventional bias recording is reproduced. The following monoflop circuit (IC8) produces a negative pulse with the occurence of the unmodulated transition of the PDM wave (length = approx. 20 µsec.). A lowpass filter extracts the DC content of the pulses. The cutoff frequencies of two consecutive stages is set to 50 Hz. The signal is amplified and an offset voltage is added (IC9).
Test have shown that the timing jitter of the incoming carrier frequency fPDM is too large for low tape speeds. A nonlinear transfer characteristic was thus necessary between the output of the filter and the input of the voltage controlled oscillator (IC1).
The first region extends from 0 < fPDM <f1. Here the characteristic exhibits a gradual slope. The influence of jitter is suppressed. In the region II (f1 < fPDM < f2) the clock frequency is constant. Timing jitter is eliminated totally. In region III the characteristic exhibits a steep slope, since jitter in this region is small in comparison to the frequency. For frequencies fPDM > fs (fs is the sampling frequency) the clock frequency is constant and the bandwidth is not increased anymore. This is implemented by the circuits around IC9 and IC10.
The control voltage is input to a voltage controlled oscillator (VCO) IC1 to produce the necessary filter clock.
IC5 and IC form an unity gain input buffer and pulse shaper.
IC5 is an AC-coupled output amplifier which feeds the output transformer located on the Connectorfield Trafo USA 1.861.777.

3.2.2.7

Timing and Test 1.861.862 (1.861.063/064/065)

It generates and supplies all timing signals necessary for digital audio, reference time, cue and time code in the D820X. Its functions can be separated into seven general blocks:

- input section
- clock generation
- varispeed-PLL
- output section.
- control
- selftest
- phaselock section

The timing and test comprises of the main board 1.861.862 and three sub-assemblies: Dual PLL 1.861.725 (two PLL on one card), VCXO 1.861.732 (for sampling frequencies 48 and 44.1 kHz) and Composide Video 1.861.720. Other VCXO cards for different sampling frequencies are available as options.

3.2.2.7.1

Input Section

The input section receives sync pulses from an external source:

- videoclock EBU 25 Hz, videoclock NTSC color 29.97 Hz, videoclock NTSC monochrome 30 Hz,
- wordclock with any of the four currently used nominal sampling frequencies (48 kHz and 44.1 kHz as long as VCXO card 1.861.732 is inserted),
- a signal from the digital input DI acccording to the professional standard set by AES/EBU, ANSI, IEC, SMPTE.
- or from a synchronizer. This latter input is nominally 9.6 kHz for the virtual sampling frequencies of 46 and 30.666 kHz.

The word- and videoclocks are selected by the external input selector and fed to the clock generation section (see next par.). The synchronizer input (T-REFEXT) is fed to the varispeed PLL and the digital input signal to an AES/EBU receiver, containing a sync detection circuit. Its output (AESSY) is also fed to the external input source selector. The digital input signal is also fed directly to the Dapro Interface board 1.861.854 where data is extracted.

3.2.2.7.2

Master Clock Generation

It is performed by two voltage controlled crystal oscillators (VCXO) with frequencies 27.648 MHz or 25.4016 MHz for sampling frequencies of 48 rsp. 44.1kHz. In order to synchronize the master timing to an external input frequency, the VCXO is inserted into a phase locked loop (PLL), consisting of two fixed dividers (by 2 and by 4), a programmable binary counter with an 18 bit address, forming a programmable divider, a phase detector (MC4044), a loop filter and a selector, which is set to a reference (an internal control voltage), as long as no external input is selected. The master clock frequency is set to (2 * 288) * fs in order to generate all possible clock patterns necessary in the recorder (one block contains 18 words of 16 bits each).
Special measures are exercised to shorten the lock-in time of the vcxo-pll especially for low input frequencies. A "presync" PLD in front of the phase detector, which sets the programmable counter and applies a common signal to both inputs of the phase comparator is only one of several circuits to obtain a a fast locking behavior. The stability of the master clock frequency is within ±10 ppm. The frequency of the external reference is required to be within the tolerance of fs ± 100 ppm, because this is the pulling range of the VCXO's. In any case, the stability requirement of digital audio equipment is specified to be fs ± 10 ppm. A VCXO-PLL is employed in order to efficiently reduce phase jitter, compared with an ordinary PLL with no crystal reference, since phase jitter can degrade the performance of some of the circuits within the PCM box. Description of VCXO: see VCXO-board (par. 2.7.1 below).
Note that the preselector PLD in front of the phase comparator generates an out-of-lock signal as long as such a condition exists (i.e. recorder set to videoclock external 29.97 Hz, but with an applied sync of 30 Hz).

3.2.2.7.3 **Varispeed-PLL**

The varispeed PLL permits frequency deviations of ±12.5% from one of the four standard sampling frequencies (fs). A programmable 12 bit binary counter is used for this purpose. Description of the PLL-circuits: see par. 2.7.2 below. It also produces 576 times fs. Due to the wide frequency range a VCX0-PLL is not practical to implement.

3.2.2.7.4 **Output Section**

Derived from the reference signal, the output section generates all frequencies and waveforms necessary in the digital part of the recorder, except for the digital output circuit. The power supply in the box is synchronized to the sampling frequency. This signal is supervised and disabled during out-of-range conditions. In such a case the internal oscillator of the power supply is freerunning at a lower frequency.

3.2.2.7.5 **Control**

Interconnection to the System Controller is by an 8 byte transmitter/receiver block, located on the board. It also feeds the Transformatter and the Run Processor with control signals. There are two bytes for varispeed and two bytes for the general configuration of the Timing and Test board.

3.2.2.7.6 **Selftest**

Since the Timing and Test board is outside of all EE-loops, it needs selftest-facilities. Therefore, clocks 1 to 9, except clock 2 (27 MHz), are tested of their existence and of their phase relationships. This is performed by forming a parity out of 9 timing signals (also the inverse of clock 6 is builded) and by comparing with a reference signal, clock 6. The test mode is initialized by the syscon and so permits most of all timing errors to be quickly recognized. The test mode can be performed any time, also during normal operation.

3.2.2.7.7 **Indicators**

* OUT-OF-LOCK INDICATOR (illuminated when out-of-lock)

3.2.2.7.8 **VCXO 1.861.732/701/702**

This board supplies the master clock frequencies in internal mode from two voltage-controlled crystal oscillators (VCXO) and forms a VCXO-PLL when the recorder is in slave mode, with wordclock, videoclock or digital input. The pulling range of the VCXO's is approx. ± 100ppm, ensuring that the speed or sampling frequency offset should be tolerable, during an interruption of the sync source (safety condition). Another benefit from using a crystal over an ordinary PLL is that its absolute stability is better. This is of major concern, since the sampling frequency stability is required to be better than ± 10ppm in digital transfer applications.

IC4 switches between internal or external control. In internal mode, a reference voltage, formed by voltage divider R11 and R12, is applied to the adjustment terminal of the VCXO's. One of the VCXO's is then selected by IC5 and its output is the master clock frequency (576 * fs).

VCXO board 1.861.732 is equipped with crystals for 48 and 44.1 kHz sampling frequencies, 1.861.701 for 48 and 44.056 kHz and 1.861.702 for 44.1 and 44.056 kHz. 32 kHz (* 576) is available on request.

In external mode, two different conditions exist: one with input frequencies in the sampling frequency range (wordclock, digital input), the other with very low frequency signals (videoclock), then in the half-frame frequency range (50, 59.97 or 60 Hz). In both cases the input signal and the signal from the feedback counter are applied to the phase detector IC1. Its output is smoothed with R1, C30. When a videosync source is selected, a current is injected into the summing node formed by R19 and R2. This current comes from a buffered voltage source (IC3) and is connected to the summing node via switch IC4 only for a short instant after selection. The length is defined by a monoflop circuit on the Timing + Test board. During this inizializing periode a current is added to the input of the loop filter (IC3), forcing its output to a nominal voltage. This action, together with others taking place on the digital board, are part of a patented fast

locking technique. The third order loop filters, one for low and the other for high input frequencies are selected by IC2 and their outputs applied to the inverting input of IC3. The positive input is offset with voltage divider R5 and R6. Careful bypassing and stabilization is essential for good performance.
The purpose of jumpers W1...W3 is to indicate the crystal configuration to the system controller. At this time up to four different VCXO's for four different sampling frequencies are at disposal. The jumper wires are factory inserted.

3.2.2.7.9 **Dual-PLL 1.861.725**

One part of it produces clock pulses for the digital output DO of the recorder. The PLL is needed because the frequency of the DO can not be directly derived from the master timing (576 * fs). The input frequency is (576 * fs) / 3024, and the output frequency 256 * fs. This signal is fed to the Dapro Interface board. The other part (the varispeed PLL) is inserted in series with the master clock frequency (576 * fs) after division by 3072 when the recorder is in varispeed mode. The data inputs of the feedback counters of this PLL are software controlled and under access by the user. The feedback counter consists mainly of a 12 bit counter, addressed by the varispeed word MCVASP1 (lower byte) and MCVASP2 (higher byte) from the System Controller. The output range of this PLL is 576 * fs ± 12.5% in normal varispeed mode or 576 * fs ± 30% in synchronizer mode. Both parts exhibit identical structures and part values with the exception of L2, the varispeed coil. The description below is for one part only.
It consists of a type 4044 phase detector (IC1 and IC5) and an active loop filter of second order (IC2 and IC6), formed of capacitors C3, C4, C14, C15 and resistors R4 and R14. Positive bias for the following VCO (IC3 and IC7) is provided by a reference voltage (1.5 V), applied to the positive input of the loop filter opamp IC2 and IC6. The next stage is a second order filter with unity gain followed by a passive RC combination (R7, R17 and C7, C17). The voltage controlled oscillator in ECL technology (IC 3 and IC 7) is a Motorola type 1648 with a varicap diode BB112 and an inductor as external tank circuit. The output of the VCO is connected to a high speed comparator in order to extend its drive capabilities. The supply voltages are separately stabilized and bypassed since they affect output jitter directly.
The PLL's are optimized for a wide lock range and peak to peak output jitter not exceeding 1 nsec., because both drive analog circuits with stringent requirements to jitter performance (sample & hold, deglitcher).

3.2.2.7.10 **Composite Video 1.861.720**

Purpose: it converts composite video signals (positive and negative, jumper-selectable) to half-frame sync pulses. The latter are input to the Timing + Test board to provide synchronization to video signals. All video standards are accepted (PAL, NTSC, SECAM), as well as any other square-wave signal with nominally 1 V amplitude. The board also contains a power-up reset circuit which prevents the synchronizing input of the Power Supply (signal SAMPCLK) from incorrect frequencies during the power-up phase.
The first stage of the composite video circuit consists of a linear amplifier with gain, AC-coupling and a jumper-selectable line termination (typ. 100 kohms or 75 ohms). This first stage feeds an inverter to obtain the possibility of using positive or negative signals (jumper positions n or p are indicated on the PC board). The next stage extracts the sync pulses from the composite signal. The video signals charge capacitor C3 via diode D1 from their negative envelope. The voltage is divided by resistors R9 and R10 and this voltage is compared to the video signal. Diode D2 compensates the voltage drop of D1. IC1 compares both signals (comparator function) and its output is the composite sync signal of the input. The output of IC1 charges C5 in the range of approx. -1... +6 V in the manner of a constant current source (R13) to obtain a a waveform which resembles the half-frame pulses. IC2 forms a schmitt-trigger to shape the output waveform to a TTL-compatible pulse.
The power-up reset circuit: C6 is charged during the power-on periode of the supply voltage and generates, with inverters IC2, a square-wave output low signal for approximately 700 msec.

3.2.2.8

System Controller 1.861.763 & Extended Syscom 1.861.764

Purpose:

- controls and supervises all audio functions
- forms an intelligent interface between the Master Processor (located in the tape deck) and digital audio via SSDA-bus
- enables operation and testing of digital audio via terminal or personal computer and stand-alone operation and testing of the PCM-box.

Hardware:

- microprocessor-system, based on MC6803, 2...8 K of RAM, 8...32 K of ROM
- SSDA (synchronous serial data adapter), a bidirectional serial 8 bit bus based on an MC6852 chip for communication with the master processor
- internal SCI (serial communication interface) for communication with a terminal (format: RS-232)
- sysbus interface for communication with digital audio, cue, head and panel electronics.
- back-up battery and battery check circuit
- power supply failure check and indication

Software: the program /RESET/ starts the entire system after a hard reset. After initialization of the hardware and after establishing the nucleus, every single task is started under control of the nucleus. Thereafter, reset is erased.
The nucleus is a real-time executive for multitasking programs. After start-up, the following programs are run by the system:

- /MONIT/: it allows interactive communication of the system with a terminal. It consists of 3 main modules:
  - basic monitor module: internal communication
  - monitor function modules: debug functions
  - user function modules: syscon functions
- /COMMND/: the command processor interpretes commands and controls digital audio via sysbus interface
- /SSDA/: this program package supports communication to the Master Processor. Commands from the master are exchanged with the command processor. Requests for status information is directly processed
- /REFTRK/: the reference track programm supports reading and writing of RT control-track information. Data read from tape is checked for CRC errors and processed. RT sector-addresses are fed to the time display program for display purposes.
- /TIMDSP/: the program time display adjusts all the various time informations (timer, watch, reference time, time code) to one common time base, it converts normalized time information to BCD code and transmits this to the time displays
- /LEVQUA/: to one part, this program transmits audio level information (to be displayed on the bargraphs) via sysbus from Gains Control board to the display panel. In a second part, it processes signal quality information, arriving from Codec, actualizes the quality counters (if necessary) and produces signal quality display information
- /CHANCO/: channel control. Supports keyboard entries and display on the channel control panel. It scans the keys, generates valid commands from the key codes, which are transmitted to the command processor and it actualizes the LED's according to the current status
- /MONCO/: the audio monitor control supports keyboard entries and display on the monitor panel as well as the control functions of the tape deck monitor, in a manner similar to /CHANCO/.

3.2.2.8.1

Back-up Battery and Check

The supply voltage of the RAM of the SYSTEM CONTROLLER is buffered with a lithium battery (3.4 V nom.). During normal operation the RAM is powered via diode D6 with D2 non-conducting. When the supply voltage fails, D2 conducts and retention of the RAM,s content is maintained. C38 acts as a buffer storage element when the battery is replaced. The comparator IC20 senses the battery voltage. The threshold for indicating "battery low" to the processor is 2.6 V with a hysteresis of 0.3 V.

3.2.2.8.2

Power Supply Failure Indicator, Reset Button

Functions:

- Monitoring of all supply voltages produced in the PCM power supply box (+5 VDC, 2 * 22 VDC, -22 VDC).
- Indication of supply voltage range by LED's.

Circuit Description:

This circuit is supplied by voltage K-PWRUP from the transport. Since this voltage is 24 VDC, it is first stepped down to 5 V by IC29. The voltage K-PWRUP is further regulated by IC28 to 2.0 V ± 0.1 V (adjustable with R14). This voltage serves as a reference to the comparator. The four supply voltages are monitored by one comparator each (IC33, 34). The output signals of the comparators are buffered for the controlling LED's (IC31). The output is fed back to the comparator. Both circuits exhibit a fast and stable triggering action to voltage thresholds set by the input divider of the comparator.
The remaining buffer IC is used to drive an LED which indicates normal operation of the microprocessor by flashing at a low frequency.
Test points for all voltages are provided behind the LED's. Physical arrangement:(from top to bottom)

RESET BUTTON FOR SYSTEM CONTROLLER

- MICROPROCESSOR NORMAL OPERATION (flashing)

- -20 (illuminated when within ± 1 V)
- + 5 (illuminated when within ± 0.5 V)
- +20PC (illuminated when within ± 1 V)
- +20 (illuminated when within ± 1 V)

The reset button for the system controller should not be used, because start-up for the panel microprocessor(s) is not provided.

3.2.2.9

Analog Output 1.861.751

Purpose: Conversion of serial data to analog signals, reconstruction of these signals and conditioning for the analog line output.

Features:

- self-contained board, accepting 16 bit serial data and feeding a balanced/unbalaced floating line output driver (not transformer coupled).
- true 16 bit performance, achieved by corrected high accuracy digital-to-analog converters.
- digital oversampling and noise shaping .
- reconstruction filter 7th order, together with 4th order phase compensation; 24 kHz bandwidth.
- DC response.
- software controlled gain adjustment.
- separate, buffered output, not affected by gain control, for monitoring purposes.

Functional description:

3.2.2.9.1

Receiver, Timing and Filter Interface

The board is interconnected to the Dapro Interface and receives data, clock and valid signals from there, and to the System Controller via a two byte receiver, from which it is supplied with gain control information. There is a timing section on the board, consisting of a 7 bit counter, generating addresses for the timing PROM, and a latch. This configuration controls the digital filter interface by two 8 bit shift register PAL's per cannel, the digital filter itself, the deglitcher and the latch of the correction circuitry.

3.2.2.9.2

Digital Filter

It performs bandwith expansion by a factor of four through interpolation. The interpolated samples are obtained at first by a fourfold increase of the sampling frequency through insertion of three zero values between every two input samples, and then by lowpass filtering this signal with a finite response (FIR) digital filter. This filter has 96 taps, and the 96 coefficients are each represented in 12 bits, so that an attenuation in the stopband above 24 kHz of about 50 dB results. At the filter output, the word has acquired a length of 28 bits. Rounding the 16 bit word to 14 bits for later processing introduces an error signal which is evenly distributed over a fourfold interval. Therefore the noise power in the 0...22 kHz bandwidth is four times less than in the case of a direct round-off from 16 to 14 bits. A factor of four in noise power corresponds with a factor of two in amplitude. The benefits obtained from the application of the digital filter are

- the DAC produces less "glich" energy while switching through its major transitions (MSB's)
- the reconstruction filter can be made more gentle and thus introducing less audible distortion (time smearing) than a filter with a steep stopband attenuation.

The digital filter also contains a noise shaping filter, which redistributes the noise power in such a way that the noise power in the audio bandwith is reduced at the expense of an increase in noise power outside this bandwith. A 7 dB gain in signal-to-noise ratio is obtained by this measure, which can directly be translated to an extra bit gained. The filter exhibits very low ripple in the transition band (±0.15dB) from 20...24.1 kHz.

3.2.2.9.3

Main DAC

The main DAC, operating with four times 14 bits from the digital filter in COB (complementary offset binary), receives its parallel input data from two 8 bit shift registers and latches. The five MSB's are additionally fed to the correction circuitry. The resolution of the DAC is 16 bits and its output is bipolar.

3.2.2.9.4

Main DAC Correction

In order to improve differential linearitiy, which can directly be measured as total harmonic distortion, a correction system is employed which is fed by the five MSB's. It consists of a PROM (organized 32 by 8 bits), a latch and an 8 bit DAC. The output current of the DAC is adjustable and is added to the current of the main DAC via a scaling network. The correction DAC is in a feedforward configuration with the main DAC.

In order to obtain full performance of the system, it is recommended not to change main DAC's individually, but to replace both main DAC and correction PROM. Matched sets are available from the factory.

3.2.2.9.5

Deglitcher and Transimpedance Stage

To suppress glitches occuring at the major transitions of the DAC, a sample & hold circuit is incorporated, which also performs current to voltage conversion. The stage introduces a first pole but it is dominated the (sin x)/x rolloff of the first order hold characteristic with its zero at four times the sampling frequency. The stage is designed for low noise and low distortion figures.

3.2.2.9.6

Phase Correction

The following filter is 4th order phase corrected up to 20 kHz by two second order allpass sections. A factory adjusted potentiometer ensures a constant input level of 10dBV.7 to the reconstruction filter. It is necessary because the output current of the main DAC varies by ±30% from its nominal value.

3.2.2.9.7

Filter

The reconstruction filter is a 7th order elliptic lowpass type, implemented with frequency dependent negative resistance (FDNR) stages, in order to obtain a wide dynamic range and low sensitivity to low frequency stray fields. The filter is flat up to 24 kHz and its stopband attenuation exceeds 50dB. The circuit and the associated level diagram is designed for low THD+N values (less than 0.002%).

3.2.2.9.8

Gain Control and Buffered Output

An MDAC controls the output line level in the range 0...20 dBV.7. Each board contains a 2 byte sysbus receiver for this purpose, which allows adjustments to be made from the LC-display of the recorder, from the panel(s), or from a remote processor. There is a separate buffered asymmetrical output, used in the D820X for monitoring purposes. Its output level is not affected by line level adjustment.

3.2.2.9.9

Deemphasis

This circuit attenuates high frequencies by about 10 db with time constants of 50 and 15 µsec. in the deemphasis mode. The control signal /FLEM/ connected from the Gains Control board 1.861.853 to both channels of the Analog Input and Analog Output boards.

3.2.2.9.10

Line Driver

It is designed to feed a balanced or unbalanced line fully floating without utilizing a transformer. The circuit consists of two identical stages, one driven with an inverted signal. The discrete output stage works with matched transistors for low quiescent current and low power dissipation. The THD+N values of the driver do not exceed 0.002% in the range 20 Hz... 20 kHz, measured over an equivalent noise bandwith of 45 kHz. A section of the circuit formed by L4, L5 and IC125, IC225 provides high CMRR values (better than 60 dB from 0.01..1 kHz). The output stage can drive capacitive loads up to 150 nF and its output impedance is 40 ohms. The maximum output level into 300 ohms is 26 dBV.7. The output is protected against RF fields from the outside by an LC-lowpass and a relay performs power-up and emergency mutings (controlled via sysbus, signal /DDIGITMU/ from the Gains Control board).

3.2.2.10

Power Supply 1.861.515

The functional principle of the switched power supply utilized in the D820X bases on a primary switched, pulse duration modulated (PDM) push-pull converter with half-wave rectifier.

The assembly consists of the boards - 1.861.517.81: High Voltage HV
- 1.861.518.81: Secondary Circuit SC
- 1.861.519.81: Mains Filter MF
- 1.861.520.81: Secondary Filter SF

Technical specifications:

Input voltage range	: 220 V ±15 % 110 V ±15 % with voltage selector
Mains frequencies	: 50/60 Hz w/o selector
Output voltages and currents:	1 * 5 VDC / 30 A 2 * 22 VDC / 2 A 1 * 22 VDC / 2 A
Ripple	: less than 50 mV peak-to-peak
Noise	: less than 150 mV peak-to-peak
Efficiency	: 75 %
Signal K-PWRUP, on state	: more than 20 VDC
Signal PWROK, logic high	: 4.5 V < 5 VDC < 6.5 V
SAMPCLK frequency range	: 37...70 kHz
Mains power interuption	: less than 100 msec. for full outp. power

3.2.2.10.1

Main Requirements

The recorder contains a switched power supply with a switching frequency synchronous to the sampling frequency. This way, all harmonics produced are integer multiples of the sampling frequency and will be folded to DC, if they occur between the input filter and the input to the ADC (on the Analog Input board), or between output DAC and output filter (on the Analog Output board). Due to this measure (patent pending) there will be no noise induced in the most sensitive stages of the analog circuitry and no degradation of signal-to-noise is likely to occur caused by the switching action of the power supply.

Another special requirement to be met: the supply should deliver nominal power even if the mains voltage is interrupted for no longer than 100 msec. (see description of the primary circuit).

There is a "power ok" signal /PWROK/, which indicates whether power is down or up to the System Controller and whether the 5 VDC supply is within a certain range (see specifications). This permits the syscon to save its status in case of a power failure. The primary relay in the power supply is energized by a power up voltage signal /K-PWRUP/, derived in the tape deck. All supply voltages are supervised on the syscon board with power failure detectors.

3.2.2.10.2

Functional Principle

Basically the block diagram shows a primary switched voltage supply with controlled 5 V supply voltage. Additionally, 5 auxiliary voltages are generated. Due to the low dissipation over the power transistors and the high efficiency of the transformers, a push-pull converter in a half-wave rectification circuit is utilized. This is fed directly from the rectified mains voltage. The mains voltage passes an RF filter which suppresses RFI, followed by a push-pull inverter (DC-AC converter) which is controlled via duty cycle. This inverter supplies the switched and transformed input voltage to the secondary side of the RF transformer, which also performs calvanic de-coupling of the mains voltage. The output voltages are subject to rectification and smoothing. The 5 VDC voltage is accurately stabilized to 5 V with a control amplifier. The common output inductance stores the energy of all four outputs. The winding ratios of the inductance have been carefully chosen for best stability of outputs which are not within the control loop.

3.2.2.10.3 **Circuit Description**

3.2.2.10.3.1 **Primary Circuit**

The mains voltage is fed from the three-pronged mains connector to fuse F1 and to the mains switch (relay K1) with DPST contacts. The mains switch is energized by a 24 VDC voltage /K-PWRUP/ from the transport. The RFI filter follows. Rectification and smoothing takes place over rectifier DZ1 (MF) (in bridge configuration) and capacitors C3 and C4 (HV). For 110V operation, another rectifier path is formed by the voltage selector. In conjunction with the smoothing capacitors it performes voltage doubling. The following selfinductance L1 (HV) increases the conducting angle. The two PTC resistors R5 and R6 (MF) limit the inrush current. Relays K2 (MF) is energized when UDC exceedes 230 V and R5 and R6 are shunted. The second contact enables the control circuit IC1 (HV) and the power supply starts.
The rectified input voltage is fed to the push-pull circuit. The MOS-FET Q1 and Q2 (HV) and the capacitors C3 and C4 (HV) form a bridge circuit. The DC voltage (approx. 320 V) is chopped into a square wave of 1/2 amplitude (approx. 160 V) and transformed via T1 (SC). The MOS-FET are controlled via CMOS circuits IC2 and IC3 (HV) and the two pulse transformers T1 and T2 (HV). The storage capabilities of C3 and C4 are choosen to bridge mains supply interrupts of less than 100 msec. at full output power.

3.2.2.10.3.2 **Secondary Circuit**

5 VDC supply: the AC voltages from the two secondary windings are rectified with D4 and D5 (SC), connected in parallel after the storage inductance L1 (SF), and finally smoothed with C1, C2 and C3 (SF).
Plus/minus 22 VDC is gained from the secondary windings of the RF-transformer. The voltages are rectified with D1, D2 and D3 (SC) and smoothed with filters consisting of L1 (SF), C11, C13 and C15 (SC).
Due to the coupling of the storage inductors of the three auxiliary voltages (+22 V, ±22 V) with the storage inductor of the controlled mains voltage (5 V), sufficient stability is reached also for the uncontrolled auxiliary voltages by an appropriate selection of the winding ratios.

3.2.2.10.4 **Internal Supply**

The auxiliary supply for the control circuit and for the driver MOS-FET's is derived from two AC-capacitors C5 and C6 (MF), the rectifier DZ2 (MF) and the smoothing capacitors C7 and C8 (MF). The series regulator IC1 (MF) stabilizes to 15 VDC with R7 and R8 (MF).

3.2.2.10.5 **Control Loop**

The central element of the control loop is formed by the integrated control unit IC1 (HV). It contains the following functional blocks:

- a voltage controlled oscillator which generates the clock frequency
- a pulse-width modulator
- a current limiter
- soft-start circuitry
- provision for external synchronization.

The +5 V supply voltage from the secondary side is compared to the reference voltage, generated by IC1 (SC), with +5 V as control voltage. It can be adjusted in a certain range with potentiometer R17 (SC).
IC2 (SC) is configured in pi-control loop and compares the control value (+5 V output voltage) with the reference voltage and forms a difference voltage. This is amplified, galvanically de-coupled from the secondary side with optocoupler DLQ3 (HV) and fed to the control IC. The duty cycle of the pulse width modulator is varied in order for the difference voltage to become zero and to obtain a stable output voltage.

3.2.2.10.6 **Protection Measures**

3.2.2.10.6.1 **Temperature Control**

A thermoswitch, mounted on the heatsink of the 5 V rectifier diodes senses the temperature. At a temperature of 90 degree centigrade the voltage K-PWRUP is interrupted. The mains relay opens and the power supply shuts down.

3.2.2.10.6.2 **Surveillance of Primary Voltage**

Capacitors C3 and C4 (HV) and MOS-FET's Q2 and Q3 (HV) are protected from overvoltage. Triac Q1 (HV) conducts, if an excessive voltage over zener diodes D1, D2 and D3 (HV) occurs. The primary fuse melts due to excessice current flow. The current through triac Q1 is limited by dump resistor L2 (HV).

3.2.2.10.6.3 **Current Limiting**

The primary current limiting circuit consists of the following elements:
T3, D4, D5, C16, R26, R31, IC1 (HV). Transformer T3 measures the primary current of transformer T1 and simultaneously the current through the two FET. If this current exceedes a certain value, the voltage at IC1 pin 7 (HV) raises above the reference voltage. The outputs of IC1 (HV), pins 12 and 13, are disabled and the power supply shuts down. When the current and the overvoltage at pin 7 of IC1 decrease, the power supply performs a soft start-up.

3.2.2.10.6.4 **External Synchronization**

The power supply can be synchronized externally with a signal exhibiting TTL level, via optocoupler DLQ2 (HV) (galvanic decoupling) and a pulse shaping circuit consisting of IC4 (HV). The synchronizing range extends from 37...70 kHz and must not be exceeded.
The power supply synchronizes to its internal frequency determined by the VCO (approx. 34 kHz), when the sync input voltage has logical high, or logical low, or is exhibits an open circuit.

3.2.2.10.7 **Indication and Adjustment**

* POWER ON INDICATOR
o SUPPLY VOLTAGE ADJUST

SUPPLY VOLTAGE ADJUSTMENT: measure +5 VDC voltage on the front side of the Gains Control board 1.861.853, when the board is not on an extender. Adjust this voltage with trimming potentiometer SUPPLY VOLTAGE ADJUST on the Power Supply to be within 4.8 ... 4.9 VDC. Check +5 VDC supply voltage on the System Controller board 1.861.763 (test point behind LED). It should be within 5.1 ... 5.3 VDC.

3.2.3 Heads and Cage Electronics

3.2.3.1 Track Geometry and Track Assignment

The bottom side of the heads, facing the die cast chassis, is designated the reference edge, from which the tracks are counted in rising order and the precision hight adjustments are made. The tape is forced to run on this edge. There are 12 tracks per head, 8 main tracks for digital audio and 4 auxiliary tracks. Their location and assignment is stated below:

track 12	aux 4	left or (left + right) cue channels
track 11	aux 3	right cue channel or auxiliary data
track 10	digital 8	CH2, track B, twin track
track 9	digital 7	CH1, track B, twin track
track 8	digital 6	CH2, track B, original track
track 7	digital 5	CH1, track B, original track
track 6	digital 4	CH2, track A, twin track
track 5	digital 3	CH1, track A, twin track
track 4	digital 2	CH2, track A, original track
track 3	digital 1	CH1, track A, original track
track 2	aux 2	reference track (time)
track 1	aux 1	time code

An overview of the track width according to format (*) and implementation in the D820X:

Type of track	Digital	Auxiliary	
Write track width	400	460	
MP track width (*)	230	290	(min. value)
MP track pitch (*)	520	580	(min. value)
Read track width	170	210	

All values in micrometer (µm).

Some of the tolerances (height from reference edge to reference line on head, azimuth, etc.) have to be adjusted to tolerances of 1 µm. Probably the most crucial aspect in head adjustment is to maintain good head-tape contact. The radius of the heads, the wrap angle and the actual position of the gap relative to the contact area have to be carefully optimized. After mechanical adjustment, the electrical parameters are evaluated. Record current for example, is a tradeoff between best frequency response and best overwrite behavior.
Mechanical and electrical head engineering is one of the most important aspects for successful production of digital tape recorders. A considerable amount of technical know-how and costly equipment is needed.
It is therefore strongly recommended not to re-adjust a factory set headblock, but to ship suspect headblocks to the nearest representative, where they will be replaced.
Also not recommended is relapping or other polishing measures.

3.2.3.2 The Function of the Heads

There are two heads in the D820X: a thin film type write head to the left side and a (currently) bulk (ferrite) read head to the right side. The single heads are easily visible on this type due to the cut-out structure of the head surface.
There is no erase head. Old recordings are simply overwritten. And there is no analog record/playback/erase head. Since the D820X uses PDM modulated auxiliary tracks (time code and cue) their recording spectrum matches that of the digital tracks and an in-line head configuration can be used. Among other benefits, this makes the headblock more robust, because the tolerances are better controlled.
The two heads are between two precision guidances.

No sync record or playback head is used. Due to its very strong error protection, the twin recording format supports hard punch-in and out at every place on the tape. The recorder performs a crossfade over such a place. The old recording is electronically faded out and and the new faded in at a constant rate. In the present implementation the fading is supplemented by a filtering action (crossfiltering).

3.2.3.3 **Cage Electronics: Description of Boards**

3.2.3.3.1 **Head Preamplifier 1.861.807**

The digitalaudio signals from the read head coils are amplified in two stages:
a) by means of a step-up transformer. The transformer provides nearly ideal amplification without degrading the signal-to-noise ratio and it also transforms the impedance of the head in order to obtain noise matching.
b) an active amplification stage, consisting of a discrete FET input stage which exhibits an optimum noise figure over the considered spectrum range, and a following opamp stage in inverting configuration. Both stages together work in non-inverting mode, with the lower frequencies limited by a capacitor in the source of the transistor and by the input transformer. The positive input of the opamp is connected to an offset voltage. Damping of the head - transformer - input impedance network is controlled by a resistor parallel to the secondary windings. Its purpose is to ensure linear phase in the used frequency range and at the same time not to attenuate the signals from the read head.
The head amplifier for the auxiliary tracks consists of a discrete amplifier stage, implemented with parallel connected bipolar transistors. For the cue tracks (aux tracks 11 and 12), where good signal-to-noise performance is necessary, four transistors are connected in parallel. An input capacitor prevents the head from magnetization and limits the lower frequency spectrum.

3.2.3.3.2 **Playback Amplifier 1.861.808**

The digitalaudio signals are first amplified by a non-inverting stage with AC-coupling and then differentiated a second time (the first differentiation is performed by the read head itself). The technique to perform second differenciation uses a delay network (allpass) and not an ordinary RL or RC combination such that the output signal amplitude is no longer in direct proportion to the signal frequency. The output voltage caused by high frequency noise is limited by this configuration. The delayed signal is passively subtracted from the input signal. A linear phase response for all relevant frequencies of the modulation code is maintained.

Auxiliary track 1 (time code): three amplifier stages in inverting configuration are connected in tandem. The gain of the middle stage is reduced at high tape speeds (more than 50 cm/sec.). Resonators follow which are changed according to the tape speed and the utilization of modulation or not. This circuit performs equalization of the waveform. The clipping circuit maintains adequate signal-to-noise margin for signals with long transition distances. After a differential driver stage the time code is fed to the TC Analog IF card 1.861.770.

Auxiliary track 2 (reference time) is processed in a similar way. Here only one resonator is employed because the the playback frequency range is limited. After the resonator/clipper arrangement the zero-crossings of the signal are detected by means of a comparator with hysteresis and fed to a differential line driver for further processing on the RT/TC Codec 1.861.861/761.

Auxiliary tracks 11 and 12 (cue or aux data): two amplifier stages in inverting configuration are connected in series, the gain of the second stage is reduced at higher tape speeds. A differential amplifier for each track feeds the signals to the PDM Demodulator 1.861.812.

3.2.3.3.3

Detector 1.861.809

Its board space is occupied by four functional blocks:

- the syscon receiver/transmitter, which receives bytes 11H (mostly SAFE/READY signals), 17H (commands for the Playback Amplifier) and 13H (the record current value) and it transmits the key settings of the Tape Deck Monitor.
- an MDAC section for software control of the record current. The MDAC (multiplying digital-to-analog converter) receives parallel data from the system controller and multiplies this value with the reference voltage applied to pin 15. The unipolar output current is converted to a voltage and fed to the Write Amplifier 1.861.803.
- the detector for the digitalaudio tracks, consisting of two active linear phase lowpass filters (second order each) which perform a slight integration of the pulses and limit high frequency noise, plus an ac-coupled crossover detector (comparator) with hysteresis for all eight tracks.
- two multiplexers to accomplish EE-loop 1. Each multiplexer handles one channel. The output signals from the detector and from the Write Amplifier are input to the MUX. Its outputs are connected to a differental line driver for further processing (equalization, demodulation) on the RUN Processor board 1.861.860/760 located in the box.

3.2.3.3.4

Write Amplifier 1.861.803

Digitalaudio data are input to IC1 (signals WRDOUT and WRDIOUT) together with block- and wordsync and wordclock. The data are demultiplexted from trackserial to trackparallel format in IC4. IC2 provides the necessary timing information. The parallel data are directly input to the positive and negative line driver IC (IC12...15 and IC18...21). The driver circuit (not the IC) is a bridge configuration formed by the collector resistors R9...32 and the output transistors in IC11...22 on each side with the head in-between.

An enable signal is fed to the second input of each line driver IC, causing its output to permanently fluctuate between on and off states during the logical high phase of the input signal. The on-off states are approximately 120/800 nsec. This pulsation of the recording current is known as "pulse train driving". It saves energy and improves crosstalk in the head, since the start incidents of the pulses for adjacent coils are timely staggered. IC3 generates the chopping pulses for the digitalaudio tracks.

With the exception of aux track 2 (reference time) the auxiliary tracks are treated slightly different. Their data is input to line receiver IC6. The (PDM) waveforms for time code and cue are asynchronous to the timing for digitalaudio. In order not to reduce resolution and consequently increase jitter and noise, the PDM waveforms are exactly reproduced by a circuit which inserts pulses between those obtained with the timing for digitalaudio, exactly at the location of the PDM transitions. IC7, 8, 9 are responsible for this operation.

The SAFE/READY signals from the System Controller are input to IC27 and synchronized with blocksync.

The digitalaudio tracks in parallel, non-pulsed form are fed to driver IC10 to be output to the Detector board for EE-loop 1 application.

The remaining parts on the board are merely voltage regulators and decoupling elements. IC23 with Q2 and Q1 form a series regulator for the recording voltage of the main tracks and reference time (RT). IC24 and IC25 do the same for cue and time code tracks respectively. The exception is that input of IC23 is a software controlled voltage from the Detector board. K1 is the mastersafe relay for cue and time code and K2 for the main tracks and RT. Both relays disconnect the power supply voltage from the record driver IC's in MASTERSAFE mode.

The test point/adjustment section:

```
* * *_____ _____ * *  ___ ___ ___ ___  **********
TP2 TP3 TP5 R35  R36  TP1 TP4  P5   P6    P3

TP2: RECORD VOLTAGE FOR CUE TRACKS (AUX 3, 4)
TP3: RECORD VOLTAGE FOR TC TRACK  (AUX 1)
TP5: GND

R35: RECORD CURRENT FOR CUE TRACKS (AUX 3, 4)
R36: RECORD CURRENT FOR TC TRACK  (AUX 1)

TP1: RECORD VOLTAGE FOR MAIN TRACKS (RT NOT INCLUDED)
TP4: GND

JUMPERS:              P3:
  INSERTED      NOT INSERTED       **********
------------------------------------ PIN 13   1
P5  RUN 9 (64 kHz)  RUN 3 (192 kHz)
              PIN 1: TRK1 (TC)
  RIGHT POSITION  LEFT POSITION     PIN 2: TRK2 (RT)
------------------------------------ PIN 3: TRK4 (DIG. 1)..
P6  HDM-1 DATA    RUNS (SEE P5)     ...PIN12: TRK12 (CUE L)
```

3.2.3.3.5

Tape Deck Monitor 1.861.802

This board is inserted when the D820X contains no monitor panel.
Its main building blocks are two identical push-pull amplifiers which drive the internal speaker and the headphones. The input signals MONTR1 and MONTR2 pass an AC coupling and a stereo potentiometer to adjust the output level. The two signals can be added by switch IC1 to obtain a mono signal when no headphones are connected (signal PHOCON removed from ground by the phones connector). Additionally, the gain of summing amplifier IC2 is reduced by 6 dB in mono mode. The signals are applied to the output driver stages (IC3 and Q1...4). These are non-inverting drivers in class a/b mode. The gain is set by R13, 14 and R24, 25 respectively. Bias for the push-pull drivers is provided by the R16, D3, R20 arrangement (left channel). The speaker is muted when the phones are connected by Q5, Q6 and K1, or by the System Controller (signal ITDSMUTE) by Q6 and K1. The remaining inverting amplifier (IC2) is only necessary to obtain identical polarity for both outputs, because the other part of IC2 (the summing amplifier) is also in inverting configuration.
Signals MON1...5 transmit the state of keys S1...5 and are connected to the Detector board. The functions and the software relationships are defined in the list "Communication Between Syscon and Hardware" in vol. III of the D820X manuals.

3.2.4 Rackelectronics (PCM-Specific)

3.2.4.1

Master and Interface to Syscon

The Master Processor 1.861.818, located in the left hand side of the tape deck rack is the top level processor in a hierarchy of processors. All communicate by means of an SSDA (synchronous serial data adapter) protocol and associated hardware. Each slave is permitted to transmit on request from master only (the single exception is the command "XON", after resynchronisation). In order to check the communication, the master sends SRQ (service request) temporarily, which is answered by the slave with ACK or NAK (acknowledge, no acknowledge) and the following status information. The slaves also check communication independently. Their status byte is set accordingly. The reaction to several invalid attempts for communication by the master is an error message, displayed in the LC-display. The slaves protect their environment as good as possible (i.e. the transport processor sets the transport in stop mode, the System Controller goes into save mode, etc.).

3.2.4.1.1

Master Processor 1.861.818 (version -22 up)

Purpose: the master MPU performes central control and supervising functions. It receives commands from

- the internal keyboard
- an external parallel keyboard
- an external serial keyboard
- the ES interface

and distributes commands to

- the System Controller 1.861.763 (see par. 2.8)
- the Tape Deck Controller 1.820.781
- the LED-display
- the LC-display

and stores most of the parameters and status information

Hardware:

- microprocessor 6803 with 56K of ROM and 8K of RAM
- SSDA (synchronous serial data adapter) for communication with the System Controller
- SSDA-bus for communication with the Tape Deck Controller
- SSDA-bus for communication with the built-in synchronizer (optional)
- a watchdog, controlling the processor
- keyboard/display interface (Intel 8279) for all lamps, the 7-segment LED display and for the keyboard
- 2 by 20 character LC-display
- an a/d converter for the shuttle control
- a counter with light barrier for the cue wheel
- remote keyboard/display interface for parallel and serial remotes (RS-232, Studer)
- the SMPTE/EBU (ES-bus) interface
- an RS-232 interface for test and development purposes with monitor.

Software:

- similar to the program of the System Controller, the software for the Master Processor is written in a real-time multitasking environment controlled by a kernel (/NUCLEUS/)
- the program /START/
- verifies checksum of nonvolatile RAM
- checks RAM
- checks EPROM version
- verifies checksum of EPROM's
- initializes the hardware
- initializes the program /NUCLEUS/
- starts all succeeding tasks
- stops itself
- /MONI/: a monitor program for test purposes (internal use only, LCD)
- /SHUT/: evaluates shuttle movements every 40 msec.

- /CUE/: evaluates cue-wheel movements every 40 msec.
- /KEY/: reads local keyboard (interrupt controlled)
  - decodes row/column addresses
  - assigns keys to a corresponding function
- /REMOTE/: reads serial and parallel remote controls (interrupt controlled)
  - decodes parallel/serial, row/column, or shuttle
  - assigns keys of serial remote to a corresponding function
  - evaluates remote shuttle movements
- /PWRDWN/: it controls the watchdog
  - supervises power supply voltages (important in the event of a shut-down)
  - transmits command "power down" to syscon
  - transmits command "stop" to the Tape Deck Controller
  - calculates RAM checksum
- /STAT/: coordinates audio and tape according to various statii
  - supervises different variables and modes
  - performes error handling and error display
- /SMPTE/: maintains the protocol to the SMPTE bus and acts according to its commands (not supported in the first versions)
- /LED/: calculates the segments of the 7-seg. LED display
  - activates the two lines of 8 status LED on top of the 7-segment LED display
  - the lamps inside or on top of the keys are activated according to the key assignment
  - program segment /BLINK/ handles flashing indicators
- /LCD/: drives the LC-display and
  - calculates LCD parameters
  - processes the keys "UP", "DOWN", "LEFT", "RIGHT" and "STORE"
  - performs reassignments of keys
- /SSDA SUPERVISOR/: it coordinates all SSDA routines to avoid overload with interrups
- /TD SSDA/: ensures the communication of the Master Processor with Tape Deck Processor
  - requests tape status periodically and receives it
- /AU SSDA/: ensures the communication of the Master Processor with the System Controller
  - requests syscon status periodically
- /IRQ/: decodes interrups and assigns corresponding routines
- /EXECUTE/: executes all functions according to a priority scheme
- /MONIFU/: contains all monitor functions (master monitor) accessible via terminal (see D820X manual, vol. III, section "MASTER MONITOR")
- /REMSER/: addressing and status management of monitor functions
- /SCI/: serial communication interface from processor to periphery
- /TAPE/: used for parameter backup on tape and RS-232 interface in Motorola hex format

Circuit Description:
IC17 is an 8-bit NMOS processor type MC6803-1. The control program comprising 56 K-bytes is stored in four ROM (IC5, IC16, and IC18). IC8 is a CMOS RAM with a capacity of 8 K-bytes. This RAM is buffered by a lithium battery which ensures that data are retained even after the D820X is switched off.

Note: The life of the lithium battery is marked on the battery itself. It should be replaced timely in order to prevent loss of data in the RAM when the recorder is switched off.

Addresses A0...A7 of the multiplexed data/address bus are assigned to the address bus with 8-bit D-latch IC13. The system clock E (enable pulse) is generated internally by IC17 with quartz accuracy. The binary counter IC7 generates eight reference frequencies from the inverted (IC9) pulse. The frequency of IC7, pin6, is output as clock frequency (TM-C76K) via the 8-bit bus driver (IC2) but is not used in this application

(spare). The clock signal TM-C307K (buffered with IC2) can be selected with a jumper (JS7, JS8, and JS9) from three frequencies. This signal is not used (spare).
To minimize the power consumption, the system clock E is also applied to the OE (OUTPUT ENABLE) inputs of the ROM and RAM (IC8, IC15, IC16, and IC18). IC12 blocks the RAMSL signal when the RESET signal is available. This prevents access to the RAM during the reset phase.
IC4 and IC6 combine the R/W signal with the system clock E for correct timing during read/write access.
IC14 monitors the 5 V supply and produces a defined reset pulse during power on as well after transient power failures having occurred during operation. With key S1, the system can be reset manually. With the TM-RESET signal the Master Serial Interface can also trigger a reset on the MP Unit Master.
The jumpers JS12...JS17 define the operating mode of the MP Unit Master IC17. These jumper settings are fixed.
JS1 and JS2 drive the mechanical elapsed play and record counter via port 15 and therefore have to be inserted (D820X only).
The address decoder IC11 (two 2-bit binary decoders) produces chip select signals from addresses A13, A14, and A15 for the ROMs, the RAM, and also supplies the enable signal for IC3. IC3 is a bidirectional data bus buffer, the direction of which is determined by the read/ write signal R/W. An additional address decoder IC5 (3-bit binary decoder) produces select signals TM-SL2...SL7 depending on the addresses A10...A15. The select signals TM-SL2...5 are used for the interface assemblies which are addressed by means of memory mapping (see Fig. 3.1.2).
The control bus is buffered by an 8-bit bus driver (IC1) and one of the gates of IC6. JS3, JS4, JS5, and JS6 are inserted and connect the signals TM-BUSSW and TM-DRENB to the serial interface.
IC12 buffers the serial inputs/outputs for a terminal.
IC2 buffers the address and clock signals as well as the reset for the peripheral devices.

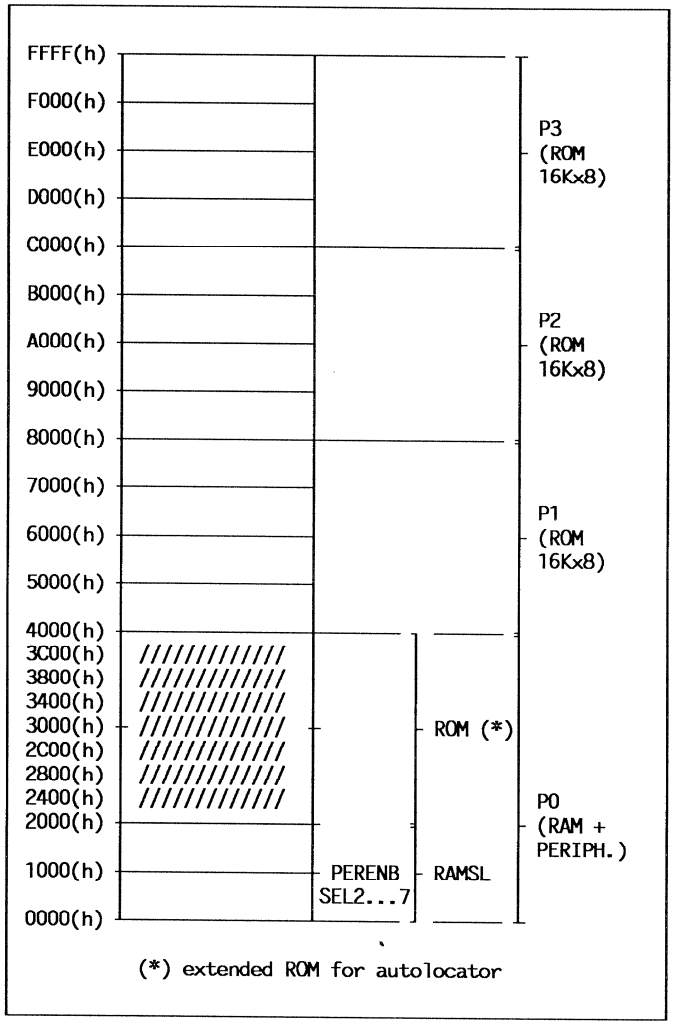


Fig. 3.1.2 Memory Map

The 8-bit data bus of the MP Unit Master is connected directly to the SMPTE/EBU Bus Interface, the Parallel Remote Interface, the Tape Deck Display Driver, the Master Periphery Controller, and the Master Serial Interface. However, the 4-bit address bus is directly connected only to three assemblies. The same applies to the system clock (TM-ENB), the write/read signal (TM-RW), and three of the five select signals (TM-SL2, TM-SL3, TM-SL6). For the other two assemblies these signals are buffered and output via Master Serial Interface. The same applies to the required select signals TM-SL4 and TM-SL5. The MP Unit Master consequently has direct access to these five assemblies. The assignment of the select signals is as follows:

TM-SL2 → Master Serial Interface
TM-SL3 → SMPTE/EBU BUS INTERFACE
TM-SL4 → TAPE DECK DISPLAY DRIVER
TM-SL5 → Parallel Remote Interface
TM-SL6 → MASTER PERIPHERY CONTROLLER

To ensure that the MP Unit Master services an interface request as quickly as possible, interrupt processing method is used. For this purpose an interrupt decoder has been integrated in the Master Serial Interface. All external interrupt requests (TM-SEIR, TM-REMIR, TM-SHIR, TM-KBIR, AND TA-AUIR) are transmitted to this assembly. On request the latter outputs an interrupt (TM-IRQ) to the MP Unit Master. Via the decoder the MP Unit Master can now determine the unit that needs to be served more quickly than would be possible in polling mode.

The power-on reset of the MP Unit Master (TM-RESMP) is transmitted via the Master Serial Interface, from where a reset (TM-RESET) is also initiated when the MP Unit Master does not correctly process the program because of a malfunction.
The two serial lines (TM-RX and TM-TX) of the MP Unit Master are not used by the SMPTE/EBU Bus Interface. They are intended for traffic via RS232-ASCII interface, e.g. to a terminal.

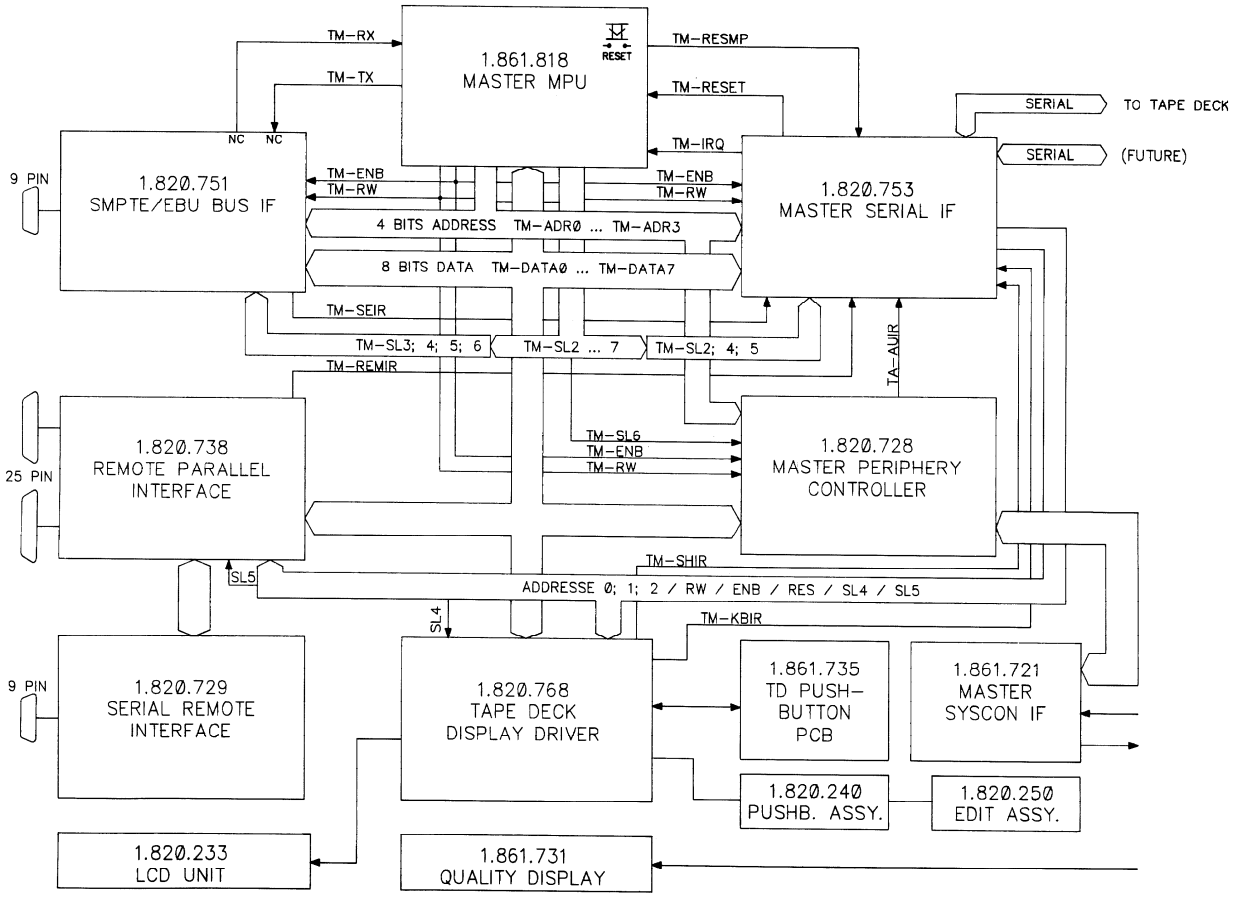


Fig. 3.1.1

3.2.4.1.2 **Master Syscon Interface 1.861.721**

It serves two purposes:

- it provides an SSDA link from Master Processor to System Controller with balanced lines according to RS-422.
- it buffers signals T-REFINT, the servo control signal, originating in the RT/TC Codec board, and the signal T-REFEXT, derived from an internal or external synchronizer. This signal is fed to the Timing + Test board.

3.2.4.1.2.1 **Implementation**

The main data bus in the tape deck, which is controlled by the Master Processor, is connected to an SSDA chip (MC68A52), together with an address bus. The IC interfaces this bus and SSDA bus with three transmitting signal lines:

- TX, the serial transmit data output line
- CLK, the transmit clock used for clocking of transmitted data. The transmitter shifts data on the negative transition of the clock.
- DTR, the data terminal ready output, serving sync purposes.

Two receive lines are provided:

- RX, the receive data line, a high impedance TTL input, through which data is received in a serial format
- CTS, the clear-to-send input, providing a real-time inhibit to the transmitter section.

All SSDA lines are interfaced with RS-422 drivers and receivers. The remaining signals T-REFINT and T-REFEXT also are interfaced according to RS-422, for high noise immunity.

3.2.4.2 Cue Track Electronics

3.2.4.2.1 General Information

The main purpose of the cue track(s) is to permit the reproduction of audio information at cue speeds (approx. 1/5 to 5 times nominal speed) for manual search of edit points. The input of auxiliary track 3 is accessible by the user and may contain additional (low speed) data for CD subcode or other applications. In the D820X PDM (pulse duration modulation) is employed for the recording of the cue (and time code) tracks, which allows to use an in-line head configuration (no separate head assemblies). With this method better alignment with the other tracks is obtained and no crosstalk of erase or bias frequencies could degrade the reproduction chain.

3.2.4.2.2 PDM Modulator 1.861.811

A digital-to-analog converter (IC1) receives two 14 bit words per sampling periode, converting from PCM to the analog domain. It is operated in multiplex mode and the current output is alternatively fed to a sample and hold circuit per channel (IC3) in order to eliminate different time delays of the cue tracks (important in sum mode). A following de-emphasis circuit (IC3) is inserted only, when emphasis has been applied to the main channels, otherwise it is bypassed. It provides complementary time constants to the emphasis circuit used for the digital audio channels (50 + 15 µsec.).
The signal is then reconstructed by an active Tschebyscheff filter of order 3 (IC4) with 1 dB ripple and a cutoff frequency (-3dB) of 15 kHz. Analog compression is then applied. It is implemented with a commercially available IC (NE 570, IC4). Its internal gain cell obeys a 2:1 ratio. The dynamic characteristics are adjusted for an attack time of 3 msec. and a release time of 13.5 msec. This is a good compromise between good audio quality and low static signal distortions. The major criteria for audible quality are low distortion at low frequencies (pumping effect) and sufficient suppression of overshoots of high frequency signals at both extremes of the audio spectrum.
The analog modulator is supplemented with emphasis (IC 6) in order to suppress tape noise, because companding alone is not sufficient. The 6 dB per-octave boost follows closely CCITT recommendation J17 but instead of applying this rise between 477 and 4134 Hz, the frequencies 500 Hz and 5 kHz have been chosen to obtain an even greater boost. The greatest benefit from emphasizing high frequencies can be gained at low tape speeds, where the output voltage from the read head is minimal.
Two cue channels are provided, one of them may be used for recording auxiliary data (labels, subcode, user data, etc.). The remaining channel will then contain a mix of the main channels (aux4mix mode). For this purpose, an adding stage is required.
IC6 operates as an adder for both channels in order to obtain a mono signal in aux4mix mode or as a simple buffer stage in stereo cue mode. After this, the signal is converted from analog to PDM by a ramp type converter (IC7 and 8), where the trailing edge is modulated. The carrier frequency $fc = 1/2T$ (T = sampling periode) and the modulation index m were chosen to obtain a large signal-to-noise ratio, to match the shortest distance between two flux changes (T min) with T min. of the main digital tracks ($2fc/(1-m)$ = approx. 192 kHz) and to extend the bandwidth of the recorded signal to 10 kHz. In order to separate the baseband from the lower sideband, fc should be greater than ca. 40 kHz.
Fc was chosen to be identical to the sampling frequency and the modulation index was set at 0.7.
The modulator will exhibit overload conditions due to emphasis and finite response time effects (attack time of the compressor). When overload occurs, the PDM waveform will remain at the previous level. After demodulation the signal will be clipped. When this happens for a longer periode of time, the filters in the demodulator limit the bandwidth to its minimum value, thus exhibiting a "distortion friendly" behavior. Tests have shown that this very rarely happens with normal program material.

3.2.4.2.3

CUE/PQ Delay 1.861.816

The complete cue recording chain, consists of three main blocks: a digital delay to compensate the average encoding delay of the main (PCM) channels, the modulator itself and the write electronics. The purpose of the delay is to align cue track information with digital audio information according to rules specified in the format.
Two 16 bit serial data words are converted to parallel in IC6 and IC7 and latched in IC8 and IC9. The data is delayed in RAM's IC10 and IC11, latched in IC2 and IC3 and fed in parallel form to the PDM Modulator (signals DP0...DP15). The delay amounts to 3996 words or 166.5 blocks for the version with symmetrical crossfade (1.861.816.23 up), or 3228 samples (134.5 blocks) for the version with asymmetrical crossfade (1.861.816.21/22).
The addressing of the RAMS's is performed by a 12 bit counter IC12...14 (in the version -23 two PLD's IC12 and 14 are used) and the entire timing for the PDM electronics is carried out with an 8 bit counter (IC19 and IC20), a 256 by 8 PROM (IC18) where the actual timing signals are programmed and a latch (IC17).
The auxiliary 3 input (XLR) at the rear side of the transport is connected to transformer T1 and R6 for galvanic decoupling and impedance matching, terminated with IC4 and a resistor R5 and fed symmetrically to the PDM Modulator and the PDM Demodulator (EE-loop) via line driver IC5. The driver is enabled with signal IMON/STE.

3.2.4.2.4

PDM Demodulator 1.861.812

One of two inputs to the Demodulator is selected with IC7: a direct path from the PDM Modulator (EE-loop and INPUT mode) provided by a symmetrical-to-asymmetrical stage and the reproduce path. The latter begins also with a symmetrical-to-asymmetrical stage (IC1) and a switchable resonator and clipper. The resonator performs differentiation to a limited degree due the resonator characteristics and integration simultaneously. The signal waveform is amplified in the operating frequency range by the resonator and clipped symmetrically by diodes D1, D2 (D22, D23). The resonance frequency is switchable to cover the specified speed range for the cue tracks (210 kHz for tape speeds from 2 to 50 cm/sec. and 460 kHz for tape speeds from 50 to 200 cm/sec., with quality factors of 0.71 and 1.6 respectively).
The output signal of switch IC7 is connected to two different circuits. The first is the actual PDM demodulator, consisting of of a fixed and a variable (switched capacitor) lowpass filter in series. The cutoff frequency fc of the variable filter is controlled by a signal which exhibits a frequency fCNTL proportional to the tape speed and in turn to the PDM carrier frequency fPDM (fCNTL = 50*fc). The filter stages are followed by a deemphasis stage (IC4) and an expander (IC13, IC5) to restore the original dynamic range. The deemphasis circuit is only complementary to the preemphasis circuit at equal tape speeds. When a tape is reproduced with a higher tape speed relative to the tape speed during recording, an accentuation of of the high frequency content results and at lower tape speeds an attenuation of of the low frequency content in the spectrum. This generally enables improved audible cueing performance. The second circuitry connected to the output of IC7, an integrator, is necessary to adequately reproduce unmodulated recordings. It contains a trimming potentiometer at its output to match the playback level to the level obtained with modulated signals. IC6 selects between modulated or unmodulated playback.
Track AUX3 exhibits one difference to the description given above: IC3 not only provides playback of unmodulated recordings (integration) but also acts as a comparator with fixed hysteresis in AUX4MIX mode (AUX3 then carries data).

3.2.4.2.4.1

Sync Extraction

The filter clock signal is derived from AUX4 track only, because it is a dedicated track for cueing applications. The first part of the circuit comprises of a comparator (IC10) with adjustable hysteresis. The following monoflop circuit produces a negative pulse with the occurence of an unmodulated transition of the PDM waveform (length = approx. 20 µsec.). A lowpass filter extracts the DC content of the pulses. The cutoff frequencies of two consecutive stages was set to 50 Hz. The signal is amplified and an offset voltage

is added. The output voltage which is proportional to the tape speed is in the range -2.6 ... 7.5 VDC after amplification.
The timing jitter of the incoming carrier frequency fPDM is too large at low tape speeds. A nonlinear transfer characteristic is necessary between the output of the filter and the input of the voltage controlled oscillator in order to obtain stable clock pulses. The transfer characteristic is shown in fig. nnn.
The first region extends from 0 < fPDM <f1. Here the characteristic exhibits a gradual slope. The influence of jitter is suppressed. In the region II (f1 < fPDM < f2) the clock frequency is constant. Timing jitter is eliminated totally. In region III the characteristic exhibits a steep slope, since jitter in this region is small in comparison to the frequency. For frequencies fPDM > fs (fs is the sampling frequency) the clock frequency is constant and the bandwidth is not increased anymore.
The behavior described above is obtained with circuitry between monoflop (IC14) and VCO (IC15). In the range -2.6V<Uo<0.5V (Uo=voltage at IC5, pin 8) diode D12 is not conducting and switch IC8 is set to pin 5. R37, 38, 39 determine the slope of the curve in this region. For a slope of approx. 1/3 of that to be obtained in region III, the value of R37 should be approx. 2*R38. R38 is variable and enables adjustment of the curve according to a specific VCO, together with an adjustment of a constant voltage which defines the lowest frequency of the VCO. In the range 0.5<Uo<Uref (Uref=voltage at IC8, pin 6 and 8) diode D12 is conducting and switch IC8 is still set to pin 5, since the input voltage to comparator is negative as long as Uo<Uref. Uref is then constant (region II). When Uref<Uo, the contact between pin 5 and pin 8 within switch IC8 is closed (the parallel contact is opened) and the output voltage of IC8 (Uref) is equal to Uo, the output voltage of IC5, pin 8.

3.2.4.2.5 **PDM Control 1.861.813**

It contains a standardized 8 byte receiver and transmitter and supplies cue electronics and tape deck signal quality display. The receiver is formed by IC15 (line recivers for addresses, clock and data), IC8 (address decoder), IC7 (3-to-8 line decoder) and latches IC1, 2, 3, 4, 5 to store 5 different bytes received from syscon. Data is converted from serial to parallel in IC6.
The transmitter exhibits a similar structure with IC10 as address decoder and IC9 as 3-to-8 decoder. Latch IC12 stores data to be fed to the syscon (the present bit only) and its parallel output data are converted to serial with IC13. Line driver IC14 is enabled only when requested by the syscon.

3.2.4.3 **Monitoring**

3.2.4.3.1 **General Information**

3.2.4.3.2 **Analog Routing 1.861.814**

3.2.4.3.3 **Tape Deck Monitor 1.861.802**

Refer to par. 3.2.3.3.5

3.2.4.3.4 **Monitor Panel 1.861.365**

Refer to par. 3.2.5.4

3.2.5 Panels and Displays: Description of Boards

3.2.5.1 **Display Interface 1.861.817**

Its purpose is to buffer the sysbus lines to the outside world of the recorder (connector "external display panel"). It therefore consists of line receivers and drivers (IC1, 2, 3, 4) and an address decoder for addresses 6H (DP TX), CH (CCP), DH (MP), EH (External DP) and FH. The decoder is built as a sequencer and enables driver IC4 only when one of the above addresses is received.

3.2.5.2 **Display Panel 1.861.555**

It consists of a two-board sandwich construction with Keyboard Display 1.861.741 and Display Processor 1.861.742.

3.2.5.2.1 **Keyboard Display**

The functional blocks of the Keyboard Display:

- 18 keys for display modes and gains control
- built-in LED's indicating actual setting for user convenience
- a 10-digit LED display with instantaneous time information of four different modes (counter, watch, time code, reference time)
- a level display for the two main channels with 50 dB range; each column displays real time audio level according to the display mode choosen (input/repro)
- one LED indicating clipping of the analog-to digital converter or digital clipping action within DAPRO (4 boards)
- a signal quality display with eight LED per channel indicating type of correction or concealment, trackloss, fingerprint, muting and dataloss

3.2.5.2.2 **Circuit Description**

LED's, digits and bargraphs are driven by special LED driver IC's (IC1, 2, 3, 4). Their built-in RAM's (9 by 8 bit) are filled by the microprocessor 6803 to be found on the Display PROCESSOR board (first byte = mode, 2nd to 9th byte = data). The drivers support multiplex mode to manage 64 LED's each, with following arrangement:

- IC1: bargraphs (DL1...5), clipping LED (DL11) and signal quality LED's (DL23...30) for channel 1
- IC2: bargraphs (DL6...10), clipping LED (DL12) and signal quality LED's (DL31...38) for channel 2
- IC3: eight 7-segment displays (DL15...22)
- IC4: two 7-segment displays (DL13, 14) and 34 single LED's, some of them in blocks (DL40...57).
  The microprocessor data bus for the display is latched by IC6 when data is valid for the drivers or for the D-type flip-flop IC5. IC5 produces enable signals for four LED drivers and for two bytes used for keys. Active key signals are buffered by IC7 and fed to the display microprocessor via data bus.

The Display Processor board contains:

- a switching regulator circuit (IC22) to convert an incoming voltage (+20 VDC) to 5 VDC. Its output feeds the Display Processor and the Keyboard Display
- a microprocessor 6803 (IC1) with memory elements, such as RAM (2k by 8, IC4) and EPROM (8k by 8, IC3), including a reset circuit (IC23)
- two address decoders (IC5 and IC7)
- an interface to the sysbus (IC8 and IC9) and auxiliary circuits (IC10...19, 21)

3.2.5.2.2.1 **Circuit Description**

According to the protocol of the sysbus, the received transmission address is checked in PAL/GAL (IC12) which in turn enables the outputs of transparent latches (IC11 or IC13) when the address is valid. Its input 9 is tied to logical high voltage by a pull-up resistor. If the jumper connector is inserted, addresses EAH and ECH are valid, indicating to the System Controller that a remote Display Panel is transmitting. For a local applications the jumper is not inserted (addresses 6AH and 6CH). The latches contain keyboard data that has been managed by the microprocessor. Data is sent to a parallel-serial converter (IC10) and is output to the sysbus via line driver IC9.
Receiving addresses are checked in a similar manner by ROM (IC14), generating an interrupt signal for the microprocessor (via IC21) when the address is valid. Received data is stored (after serial-parallel conversion in IC16 and IC17) in latches IC15 and IC18.
Two encoders IC5 and IC7 are connected to the microprocessor bus to generate enable signals for RAM and ROM and for four latches IC11, 13, 15, 18 according to the selected address.

3.2.5.2.3

Software

PAL/GAL DP8BTRM : transmit address check
PROM DISADR : receive address check
EPROM DISPAN : program for levels, LED, signal quality and seven-segment display

3.2.5.3

Channel Control Panel 1.861.370

It consists of a two-board sandwich construction with CCP Keyboard 1.861.743 and CCP Transceiver 1.861.744.

The functional blocks of the CCP Keyboard:

- 17 keys for channel control functions (safe, ready, input, repro, RT Sync)
- 21 LED's indicating actual configuration
- 3 D-type flip flops driving LED's, 3 buffers for key signals and 3 resistor networks (8 * 330 ohms each) for current sourcing of the LED's

The CCP Transceiver contains:

- a switching regulator circuit IC8 to convert an incoming voltage (+20 VDC) to 5 VDC and feeding CCP TRANSCEIVER and CCP KEYBOARD
- an interface to the sysbus with auxiliary circuits.

3.2.5.3.1

Circuit Description:

Incoming addresses are checked in PAL/GAL IC2 and IC5. IC2 outputs a special code byte to data selector IC3 according to the address, if the received address is recognized as a valid receiver address for the Channel Control Panel. IC3 then enables one of three D-type flip flop outputs (IC1...3). These IC's contain received data from the serial-to-parallel converter (IC4). LED's indicate information from the outputs of IC1...3.
When a valid address has been a transmitter address, PAL/GAL (IC5) outputs a special code byte to data selector IC6 according to the address. IC5 enables one of three buffers (IC4...6) which change to transparent mode. Information is now fed from the keys to the parallel-serial converter and data is output to the sysbus driver (IC9).

3.2.5.3.2

Software

PAL/GAL CCP8BTRM : transmit address check
PAL/GAL CCP8BREC : receive address check

3.2.5.4

Monitor Panel 1.861.365

It contains

- 6 keys for monitor mode control
- 8 LED's indicating actual setting
- a sysbus interface with auxiliary circuits
- a 2-channel monitor amplifier

3.2.5.4.1

Circuit Description

Incoming addresses are checked in IC4 (PAL/GAL). It enables IC7, a D-type flip-flop, when a valid receiver address for the Monitor Panel has been recognized. IC7 drives LED's. IC4 also enables a parallel-to-serial converter (IC9) for serial in - parallel out mode, because sysbus data is received in serial form and IC7 requires it in parallel.
When an incoming address is recognized as a transmitter address, PAL/GAL (IC4) enables IC9 for parallel in - serial out mode and IC9 is ready to receive parallel data from buffer IC10. The buffer is changed from tri-state to active by PAL/GAL IC4 and is now ready to accept data from the keys. They are subsequently fed to an RS-422 driver (IC5) and to the symmetrical sysbus.
If no incoming address is valid, IC9 and IC7 are enabled and IC10 remains in tri-state.

3.2.5.4.2

Software

PAL/GAL MPRECTRM: receive and transmit address check

3.2.5.4.3 **Monitor Amplifier**

CH1/2 signals from Analog Routing board are AC-coupled with C1 and C4 and fed to volume control potentiometer R33. After another AC-coupling, push-pull drivers Q1, 2 and Q3, 4 amplify the signals from driver IC3. The signal of the left speaker is amplified by 6 dB when both channels are added.

3.2.5.5 **Signal Quality Display 1.861.731**

The signal quality display located on the tape deck receives 2 bytes parallel data from board PDM Control and drives 16 LED's via drivers IC1, 2 and 3. Assignment and coding is described in list "Communication between Syscon and Hardware" in vol. III of the D820X manuals (Servicing).

3.2.6 Transport Electronics

3.2.6.1 **Power Supply, Tape Deck Control**

3.2.6.1.1 **Overview**

The section 3.2.6 is divided as follows: at the beginning (3.2.6.1), the circuit descriptions of the general assemblies (e.g. power supply) can be found. These are followed by descriptions of the remaining electronics (3.2.6.2) and motor control (3.2.6.3).

Utilized abbreviations:	
ACIA	Asynchronous communication interface adapter
ADC	Analog to digital converter
CMOS	Complementary metal oxide semiconductor
DAC	Digital to analog converter
FIFO	First in, first out
IRQ	Interrupt request
LSB	Least significant bit
MPU	Microprocessor unit
MSB	Most significant bit
NMOS	N-channel metal oxide semiconductor
NMI	Non maskable interrupt
PIA	Peripheral interface adapter
PIO	Parallel input/output
PROM	Programmable read only memory
RAM	Random access memory
ROM	Read only memory
SSDA	Synchronous serial data adapter
VMOS	Vertical metal oxide semiconductor

3.2.6.1.2 **Power Supply Electronics 1.820.510**

Function:

- Supply of GRP32 (Switching Stabilizer PCB 1.820.790) with a filtered DC voltage (approx. 50 to 60 V), and GRP31 (Spooling Motor Supply PCB 1.820.777) with an AC voltage (approx. 35 to 45 V).

Circuit Description:

The line voltage is applied to a 3-pin power inlet (GRP01/ELM01). The insulation of the power supply corresponds to IEC65, protection category 1; the protective ground terminal is connected to chassis (GRP02/ELM01). From the power inlet the AC voltage is taken via the power switch (GRP03/ELM01), the interference suppression filter (GRP04), the primary fuse (GRP05), and the 220 V/110 V voltage selector (GRP07) to two identical power transformers, GRP08 and GRP09. Each primary winding (ELM01 and ELM02) consists of a 100 V and a 10 V winding that are connected in series (interconnection of PNT01 with PNT04 on ELM01, as well as PNT06 with PNT07 on ELM02). The 6 identical secondary windings (ELM03 and ELM04) of GRP08 are all connected in parallel and connected to GRP31/ELM02 (Spooling Motor Supply PCB

1.820.777 GRP31). These 6 identical secondary windings (ELM03 and ELM04) of GRP09 are combined in three units:

- The first unit comprises three parallel-connected windings and supplies the positive section of Switching Stabilizer PCB via the fuse (GRP10/ELM01), the bridge rectifier (GRP11/ELM01), and the filter capacitors (GRP12/ELM01 and GRP12/ELM02).
- The second unit comprises of two parallel-connected windings and supplies the negative section of the Switching Stabilizer via fuse (GRP10/ELM02), bridge rectifier (GRP11/ELM02), and filter capacitor (GRP12/ELM03). The AC voltages ACPWE-B1 and ACPWE-D1 are tapped on the input to the bridge rectifier and are also taken to the Switching Stabilizer.
- The third section comprises of the remaining winding and supplies the capstan motor control via fuse (GRP10/ELM03), bridge rectifier (GRP11/ELM03), and charging capacitor.

The three DC output voltages are approx. 50 to 60 V each, without connected load.

3.2.6.1.3 **Switching Stabilizer 1.820.790 + Stabilizer/Limiter 1.820.792**

Function:

- Producing all regulated voltages required by the tape recorder:
- +5.6 V for the logic circuits
- +15 V and
- -15 V for the audio section
- +24 V for the incandescent lamps of the tape command keyboard and the brake solenoids,
- +26 V and
- -26 V for the positioning motors of the pressure unit, as well as
- the supply voltage (+REMSUP) for a serial remote control (approx. 50 V, current limitation at approx. 1 A).

The +24 V supply voltage of the terminals for the parallel remote control and the synchronizer is produced on the Parallel Remote Interface with a preset linear voltage regulator (IC15) from +REMSUP.

Circuit Description:

- SWITCHING STABILIZER PCB 1.820.790
  By means of a voltage regulator this circuit produces +5.6 V and ±15 V from input voltages +STABIN and -STABIN. The three switching regulator components (IC1, 2, 3) are fed by one of the two linear voltage regulators for +26 V (IC103) and +24 V (IC8). IC103 and IC8 are mutually decoupled by D101 and D15. The three switching regulators operate synchronously with a clock frequency of 76 kHz (TD-C76K) which is generated by the MP Unit Tape Deck Control 1.820.785 GRP20/ELM46. This clock is checked for correct frequency by IC7.1/7.2, the parallel oscillator circuit L4/C37, and dual one shot IC6, and noise is thereby filtered out.
  - +5.6 V control:
    from +STABIN the switching regulator produces +5.6 V supply voltage. The clock of IC6/pin 5 is taken to IC1 (regulating pulse width modulator). IC1 contains the reference voltage source, oscillator (not used in this application), error amplifier, and current limiting circuit. The output of IC1 (CA/CB) controls the driver transistor Q1, and via driver transformer T1 also the switching transistor Q4. From the pulsating voltage produced with Q4 and the free-wheeling diode D22 a new mean is formed with L5 and C28. This DC voltage is refiltered with L1 and C26. The voltage fluctuations across L1 increase with rising output current and are used as information for the current limitation in IC5.2. The attack point of the limitation is approx. 7 A. The output voltage of the switching regulator can be adjusted with trimmer potentiometer R21.
  - ±15 V control:
    functions analogously; the two switching regulators produce +15 V and -15 V from +STABIN and +STABIN respectively. The +15 V regulator comprises of the

following components: IC3, Q2, T2, Q5, D23, L6, C35, L3, C30, AND IC5.1. The -15 V regulator comprises of the following components: IC2, Q3, T3, Q6, D24, L7, C36, L2, C31, and IC4.1. The -15 V regulator is wired in such a way that its output voltage is of the same magnitude as the one of the +15 V regulator (tracking mode) which means that no -15 V can be present when +15 V are missing. The reference value of the output voltage is adjusted in common with trimmer potentiometer R6.

- +24 V control:
  +24 V are produced from +STABIN with a preset linear voltage regulator (IC8).

- STABILIZER/LIMITER PCB 1.820.792
  - +26 V and -26 V are produced by preset linear voltage regulators (IC103, IC104) from +STABIN and -STABIN.
  - The supply voltage for serial remote control (approx. +50 V, unregulated) is produced from +CAPMOT. Two linear voltage regulators are used for limiting the current. IC101 is wired as a current source, the max. current is approx. 1 A. IC102 limits the input voltage of IC101 to approx. 35 V in the event of a short circuit.
  - The comparator IC100 monitors the secondary voltage (ACPWE-D1, ACPWE-B1) of the power transformer; in the event of a power failure it signals T-PWRON = LOW to both CPUs. The machine is switched to STOP and SAFE after 120 ms. If the power failure is shorter than 120 ms, the logic state of the equipment does not change.
  - The crowbar circuits comprising of Q101 and Q100 respectively monitor +5.6 V and the ±15 V switching regulators. If one of these voltages is exceeded by approximately 3 V, the corresponding triac fires and short-circuits the +5.6 V to ground and the +15 V to -15 V.

3.2.6.1.4 **Fuse/Supply Failure Detector 1.820.737**

Functions:

- Monitoring of all supply voltages in the machine (+5.6 V, +15 V, -15 V, +24 V, +26 V, -26 V, +STABIN, -STABIN, +CAPMOT).
- Indication of supply voltage availability by means of a LED.
- Message (Signal T-SUPVON = LOW on the Tape Deck Periphery Controller 1.820.762 (GRP20/ELM43), if one of the supply voltages is too low or missing.

Circuit Description:

This circuit can be supplied by three different voltages: by +CAPMOT, by +STABIN or by +26 V; the circuit remains operational even if one or two of these voltages fail. +CAPMOT and +STABIN are decoupled by D2 and D4. Since these two voltages are unregulated and can amount up to 63 V, they are first stepped down to 24 V by IC2. These 24 V and the +26 V are decoupled by D1 and D3 and are regulated by IC1 to 5.0 V ± 0.1 V (adjustable with R2). This voltage is used to supply the comparators and gates on the circuit board. In addition, it is regulated by IC12 to 2.00 V ± 0.01 V (adjustable with R47) and serves as a reference to the comparator. The nine supply voltages are monitored by one comparator each (IC4, 5, 7, 9, 11). The output signals of the comparators are AND-gated (IC6, 3) → T-SUPVON and also buffered for controlling the LEDs (IC8, 10).

3.2.6.1.5 **Spooling Motor Supply 1.820.777**

Functions:

- Supplies approx. 30 V to the Spooling Motor Drive Amplifiers 1.820.775 GRP30/33.
- Absorbs the energy released by the spooling motors during the deceleration phase.
- Limits the charging current of the filter capacitor (GRP34) when power is switched on.
- Continuously monitors the current of the spooling motors.

Circuit Description:

- Power on procedure:
  - Initially the phase angle control circuits IC2, and consequently the three parallel-connected triacs Q4-6, are blocked. The filter capacitor (GRP34) slowly charges via R52//R53//R54, however, only when the load on the output (±PSVTMOT) is minimal.
  - The output voltage (±PSVTMOT) is symmetrized by the resistors R20, 21. The differential amplifier IC4/1 derives an asymmetrical voltage from ±PSVTMOT and divides it by 10. This voltage is called +Y-SUP.
  - IC2 is supplied via ACPWM-B1...B6 and ACPWM-A2,A5. The DC supply voltage is available between pins 11 and 15.
  - Since DLQ1 initially blocks the voltages on pins 9 and 13 are identical (approx. 4 V). The Schmitt trigger with open collector output in IC2 is wired as a flip-flop (pins 5, 6, 7). Its output carries approx. 7 V across R36 because the flip-flop has been forced to this state by C9 on pin6 when the power was switched on. C9 slowly charges via R18 to UREF (voltage on pin 14 of IC2, approx. 2 V) and remains in this condition.
  - The main current flows through D4 and D5 into the base of the phototransistor of DLQ2. The phototransistor becomes conductive, pulls the control input pin 17/IC2 to low, and thereby prevents triggering of IC2.
  - As soon as +Y-SUP exceeds the voltage on pin 6 of IC3/2 (UREF2), UREF1 (node R24,26,29) is suddenly connected to pin 5 of IC4/2. This can be checked by TD-PWENB and requires active low; TD-PWENB has priority.
  - The current which now flows through DLQ1 and DL1 produces a secondary current in the emitter of DLQ1 in a sudden burst. Q1 becomes conductive and makes Q2 also conductive. Q2 remains conductive because of R23.
  - The soft start now begins because Q2 is conductive; D4, 5, and the phototransistor in DLQ2 block; the output of IC2 (pin 2) is enabled via pin 17. The soft-start time is determined by R15, 17 and C6.
  - The current across DLQ1 drops slowly. When PSVTMOT or +Y-SUP respectively attains the value (approx. 30 V or 3 V respectively) determined by UREF1 (node R24,26,29), the current through DLQ1 and the control LED DL1 has attained the nominal value. The emitter current of DLQ1 is converted to a proportional voltage in IC2 and actuates the voltage-controlled phase shifter (IC2, pin 13).
  - The control loop is now closed because the declining voltage resulting from the rising load on the output (+PSVTMOT) causes earlier triggering of the triacs and makes more power available to the filter capacitor (GRP34).
- Overvoltage protection:
  During spooling functions much power is briefly drawn from the Spooling Motor Supply. During the deceleration phase the spooling motors function as generators and consequently supply electrical energy. This energy is stored in the filter capacitor (GRP34). The voltage across the latter's terminals rises sharply. However, as soon as ±PSVTMOT becomes greater than approx. 32 V, the discrete power Z-diode (IC5, D9, Q7-9) becomes conductive. The released energy is dissipated in the form of heat. DL2 (red) turns on, DLQ2 is enabled and via pin 17 blocks the output driver of IC2 with the result that no additional power from the mains is supplied to the filter capacitor during the deceleration phase.
- Overcurrent protection
  If the voltage ±PSVTMOT drops below approx. 17 V because of an overload, IC2 is blocked via IC4/1, IC3/2, IC4/2, and DLQ1; the triacs no longer receive triggering pulses and block. In this case the voltage on IC2/pin 13 is approx. 4 V.

3.2.6.1.6

Master Serial Interface 1.820.753

Functions:

- Interface to the Tape Deck Serial Interface
- Buffering of the address bus and control bus to the Parallel Remote Interface as well as to the Tape Deck Display Driver.
- IRQ triggering in the MP Unit Master 1.820.786 as well as decoding of the interface requesting an IRQ.

Circuit Description:

IC5, a PIA (Peripheral Interface Adapter) and the two SSDAs IC6 and IC9 (Synchronous Serial Data Adapter) are integrated in the data and address bus of the MP Unit Master and permit direct access by the processor. The required address decoding is performed by IC11 (2-bit binary decoder).

Communication with the Tape Deck Serial Interface takes place through serial data transmission. The required parallel/serial or serial/parallel conversion is performed by the two SSDAs (IC6 and IC9). Data is transmitted by means of a hardware handshake. The required data clock is derived from the sy- stem clock "E" by means of frequency division with a twin 4-bit binary counter (IC12) and after buffering by IC3 (8-bit bus driver) it is input to the two units. The serial signals are buffered by IC4 (8-bit bus driver). With the two RS422 line drivers (IC1 and IC2) the control bus and the address bus are connected to the Parallel Remote Interface and to the Tape Deck Display Driver with symmetrical voltage. They also fulfill an output function, like IC5, IC6, and IC9.

Two retriggerable monoflops (IC13) must be retriggered in regular intervals by the MP Unit Master which is always the case as long as the processor executes its program correctly. In the event that a malfunction occurs or the program "hangs", a LOW pulse that reinitializes the processor (reset) is output by IC13.

IC8, IC7, IC10 and part of IC5, constitute a priority decoder for IRQ requests. For this purpose the five IRQ sources TM-SEIR, TM-REMIR, TA- AUIR, TM-SHIR, TM-KBIR as well as those of the two SSDAs IC6 and IC9 are logically combined by IC7 and IC10 with an 8-bit word from port PA (IC5) and input to the 8-to-3 priority encoder IC8. The 3-bit word on the output of IC8 (A0, A1, A2) is read via the port PB (IC5), after IC8 has triggered an IRQ. If several IRQs are triggered at the same time, the 3- bit word on the output of IC8 contains the three bits that correspond to the most significant input of IC8. Like Q1, IC3 (8-bit bus driver) also serves as a buffer.

3.2.6.1.7

Parallel Remote Interface 1.861.780

Function:

Interface between MP Unit Master and

- parallel remote control
- Serial Remote Interface board
- synchronizer port

Circuit Description:

IC3, a keyboard display interface, establishes the connection between the serial remote interface, the parallel remote control (control and acknowledge lines), the synchronizer port, and the MP Unit Master. The bidirectional data bus is connected directly to the MP Unit Master. However, the control signals for IC3 (chip select, read/ write, clock, address 0 and reset) arrive via the Master Serial Interface. These signals are brought to TTL level by the two RS422 line receivers IC4 and IC2. These signals are preprocessed for IC3 by IC7, IC8, IC1B (2-bit binary decoder) and IC2.

The eight inputs RL0...RL7 of IC3 are connected to the Serial Remote Interface to ensure that the data from the serial remote port are accepted when the signals ROW0...ROW5 (OE) of IC5 are active. But also the inputs from the parallel remote or synchronizer ports are connected to the inputs RL0...RL7 of IC3 after they have been buffered by comparators via IC10 or IC6 respectively, when IC10/IC6 are enabled by

the signals ROW6 or ROW7 of IC5. The parallel remote as well as the synchronizer ports are scanned by IC3 with the latter's outputs SL0...SL3 via the binary decoder IC5.
The outputs B0...B3 and A0...A3 of IC3 are connected by IC3 to a 6-bit D-register (IC9) and an 8-bit D-register (IC14), and are stored by the latter after the data have been accepted. For this purpose the data transfer signals L6 and L7 are decoded by IC1A (binary decoder). The outputs of IC9/IC14 are transmitted through buffers to the parallel remote and synchronizer ports.

3.2.6.1.8 **Serial Remote Interface 1.820.729**

Functions:
- Serial/parallel and parallel/serial conversion from/to the serial remote port.
- Transfer/acceptance of data from/to the parallel remote interface.

Circuit Description:
The Serial Remote Interface is connected directly to the Parallel Remote Interface and establishes the connection to the serial port.
IC9, an RS422 transceiver, establishes the connection between the serial port and the MPU IC8. The latter performs the serial/parallel conversion. The data are transmitted to the Parallel Remote Interface via IC4 and IC1. Both 8-bit D-registers are used as 1-byte memories in order to permit asynchronous transmission. For this purpose the MPU (IC8) writes the byte into IC4 and connects it via the address decoder IC2 to the output (IC4). The pulse shaper (EXOR IC3) forms a clock pulse from the T-SL0 signal, IC1 now accepts the data from IC4. With the T-OE signal these data are connected to the output of IC1 and accepted by the Parallel Remote Interface (IC3). Since the T-SLO signal is also read by the MPU (IC8) via the input P10, the MPU knows when the last data have been accepted so that it can output the next byte from the internal RAM. The data transfer is thus controlled by the MP Unit Master.
The data to be transmitted are already latched in the Parallel Remote Interface and are read by the MPU (IC8) via IC5. IC7 is a ROM whose addresses are controlled by IC6. The parallel/serial conversion is again performed by IC8, the output via IC9.

3.2.6.1.9 **SMPTE/EBU Bus Interface 1.820.751**

Function:
- Interface between the MP Unit Master and the SMPTE/EBU bus connector.

Circuit Description:
IC17 is an 8-bit NMOS microprocessor with a clock frequency of 4 MHz; the corresponding control program is stored in ROM IC16. The addresses A0...A7 are assigned to the address bus by IC15 (8-bit D-latch). IC5 (binary decoder) is the address decoder. IC18 is an ACIA (asynchronous communication interface adapter) for serial communication. This adapter is designed not only for RS232 but also RS422. The driver for the RS232 output is IC3; IC11 is used for RS422. The corresponding operating mode is selected with jumper JS2. IC7 is the serial receiver; the selection between RS232 and RS422 is made with the jumpers JS5, JS6, and JS7.

	RS232	RS422
JS2	B-A	B-C
JS5	B-A	B-C
JS6	B-A	B-C
JS7	B-A	B-C

The clock required for serial output is derived from the system clock TM-ENE of the MP Unit Master via IC19 (4-bit binary counter). Two baud rates can be jumper-selected:
JS3 A-B = 1200 baud
JS3 C-B = 38400 baud for SMPTE/EBU bus or
9600 baud for RS232/RS422 interface

IC10 is a 14-bit counter that is used for detecting the break character on the SMPTE bus. Via pin11 the counter is reset by each transmitted or received signal. If signals are missing for a certain period (468.75 us or 576 E-signal pulses), IC6 outputs L level. If jumper JS8 is set to B- C, the DCD signal is produced for IC18 which means that an interrupt is signalled to IC17 via the IRQ1 line. The interrupt program of the CPU (IC17) reads the status register IC18 and a break character is detected. The corresponding software subsequently sets the bus interface to the active state.
IC4 is a dual ported FIFO chip with a storage capacity of 128 bytes. It is used as a bidirectional data buffer for exchanging information between the two MPUs.
The data are written by the MPU IC17 via IC9 (8-bit D-flip-flop) into IC4 from where they are read by IC13 (8-bit bus driver). The second port of IC4 is connected to the data bus of the MP Unit Master via IC2 (8-bit D-flip-flop) and IC1 (8-bit bus driver).

3.2.6.1.10

Tape Deck Display Driver 1.820.768
with:

PUSH BUTTON ASSEMBLY	1.820.240
▪ TAPE DECK PUSHBUTTON PCB	1.820.769
▪ TAPE DECK INDICATOR PCB	1.820.766
OPERATING ASSEMBLY	1.861.235
▪ DISPLAY PUSHBUTTON BOARD	1.861.735
LC DISPLAY UNIT	1.861.233
▪ LCD MODULE	73.01.0125
▪ LCD CONNECTOR PCB	1.820.797
▪ QUALITY DISPLAY	1.861.731
EDIT ASSEMBLY	1.820.250
▪ CUE SENSOR PCB	1.820.765
▪ SHUTTLE CONTROL PCB	1.820.776

Functions:
- Interface for display and keyboard.
- Analog/digital conversion of the analog signals from the shuttle control potentiometer.
- Evaluation of the cue sensor pulses.

Circuit Description:
The analog signal ANM-SH2 from the wiper of the shuttle control potentiometer is transformed by IC7/IC9 (ADC) to an 8-bit data word and placed on the data bus of the MP Unit Master.
The cue sensor is located in the edit assembly. The dual forked light barrier of the cue sensor supplies two TTL pulses TM-CUE1/TM-CUE2. The edge steepness of the two pulses is refreshed by two inverting Schmitt triggers (IC14) and placed on 4-bit D-register IC8. Two NAND gates (IC6) form an RS flip-flop that determines the counting direction (UP/DOWN) for two 4-bit up/down counters IC10 and IC12, based on the phase relation of the two pulses TM-CUE1, TM-CUE2, by means of EXOR gates (IC5). The register outputs of the two up/down counters IC10 and IC12 are placed on the data bus of MP Unit Master. The required enable signal is supplied by address decoder IC18.
IC21, an RS422 line receiver, transfers select signal TM-SL4 and three addresses A0...A2 to MP Unit Master 1.820.786 via address decoder (IC18). The read/write signal (W), the reset pulse (RES), and the clock (ENB) are accepted by MP Unit Master via the second RS-422 line receiver (IC22), and after logical combination are made available to IC9, IC8, and IC13.
The LC display unit is linked to the tape deck display driver by connector P4.
The keyboard/display interface IC13 establishes the connection between the MP Unit Master and the following units:

3.2.6.1.10.1

Tape Deck Indicator 1.820.766

IC23 is wired as a constant-current source (approx. 200 mA) and is used for limiting the inrush current of the incandescent lamps. The incandescent lamps are switched on by the dual NAND drivers IC1, IC2, and IC3. These are controlled by IC13 via a 6-bit D-register (IC4).

3.2.6.1.10.2

Display Pushbutton Board 1.861.735

The ten 7-segment displays (with common anode) on the Pushbutton/Display PCB as well as the LED matrix DL1.0...1.7, DL4.0...4.7, DL5.0...5.7) are controlled in multiplex mode. All segments, the decimal points, and all cathodes of the LED matrix are controlled by LED segment driver IC11. The common anodes of the corresponding 7-segment display (DLZ1...DLZ10) are controlled by the signals TM-D0...TM-D9; the anodes of the LED matrix are controlled by the signals TM-L4 and TM-L5: These signals are produced by two binary demultiplexers IC19 and IC20 based on the specifications of IC13, and are buffered by the transistors Q1...Q15.

3.2.6.1.10.3

Tape Deck Pushbutton PCB 1.820.769

The Hall-effect buttons on the Pushbutton/Display PCB are wired in a matrix. Scanning for a pressed button is performed by IC 14, an addressable 8-bit latch, in four rows (TM-EN1...TM-EN4). The TM-EN0 signal is responsible for the buttons of the Tape Deck Pushbutton PCB. The keyboard/display driver IC13 periodically outputs the five signals TM-EN0...EN4 and each time reads via its inputs RL0...RL7 the corresponding column of the keyboard in order to determine whether or not a button has been pressed. If this is the case, the IRQ TM-KBIR is triggered.

3.2.6.1.2

Remaining Tape Deck Electronics:

Consisting of:

MP UNIT TAPE DECK CONTROL	1.820.785
TAPE DECK SERIAL INTERFACE	1.820.763
TAPE DECK PERIPHERY CONTROLLER	1.820.762
TAPE LIFTER CONTROL	1.820.773
OPTO SENSOR	1.820.793
TAPE DECK COUNTER/TIMER	1.820.761
MOVE SENSOR	1.820.770
MOTOR TACHO	1.820.771
SPOOLING MOTOR CONTROLLER	1.820.760
SPOOLING MOTOR DRIVER	1.820.759
SPOOLING MOTOR DRIVE AMPLIFIER	1.820.775
TAPE TENSION SENSOR	1.820.772
CAPSTAN CONTROL UNIT	1.820.764
CAPSTAN INTERFACE	1.820.727
TACHO SENSOR ELECTRONICS	1.021.695
CAPSTAN MOTOR DRIVE AMPLIFIER	1.820.774

Functional description according to the block diagram Fig. 3.1.5:
The 8-bit data bus, the address bus, and the control bus are connected to five periphery assemblies. An address decoder in the MPU TD Control produces the select signals that are assigned as follows:

TD-SL2 → not used
TD-SL3 → TAPE DECK PERIPHERY CONTROLLER
TD-SL4 → SPOOLING MOTOR CONTROLLER
TD-SL5 → TAPE DECK SERIAL INTERFACE
TD-SL6 → TAPE DECK COUNTER/TIMER
TD-SL7 → CAPSTAN INTERFACE

When power is switched on, a reset (TD-RESMP) is output to the Tape Deck Serial Interface: The Tape Deck Serial Interface is reset and supplies a reset (TD-RES) to the remaining four assemblies.
Communication between MPU Master Control and MP Unit Tape Deck Control is performed via Tape Deck Serial Interface by means of a serial link to the Master Serial Interface.
An interrupt can be triggered by the Tape Deck Serial IF, the Tape Deck Counter/Timer, and the Capstan Interface. These are ORed and serviced in polling mode by the MPU.
Communication between MP Unit Tape Deck Control and Capstan Motor Control Unit takes place via Capstan IF. For this purpose the two data buses TD-DATA and TC-DATA are interconnected via two PIOs. Communication is performed in IRQ mode.

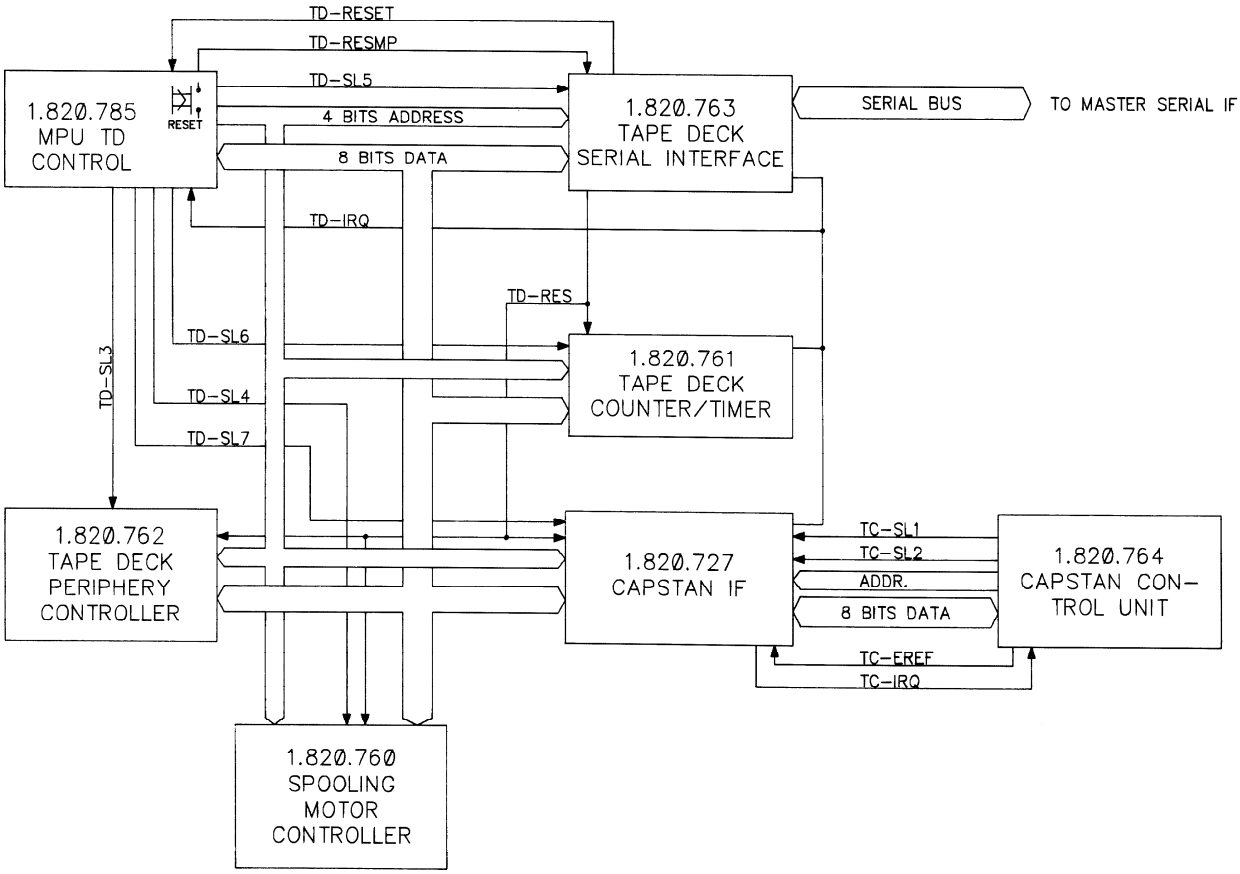


Fig. 3.1.5

3.2.6.2.1

MP Unit Tape Deck Control 1.820.785

Functions:

- Slave processor of the MP Unit Master for function-oriented control of the two spooling motors and the capstan motor.
- The status field of the tape deck is buffered in the RAM and transmitted on request to MP Unit Master.

Circuit Description:

IC17 is an 8-bit NMOS processor type MC 6803-1. The control program comprising 48 K-bytes is stored in three ROMs (IC15, IC16, and IC18). IC8, a CMOS with a capacity of 2 K-bytes serves as RAM.
8-bit D-latch IC13 assigns addresses A0...A7 of the multiplexed data/address bus to the address bus. System clock E (Enable pulse) is generated internally by IC17 with quartz accuracy. Binary counter IC7 generates eight reference frequencies from the inverted (IC9) pulse. The frequency of pin6 (IC7) is output as clock frequency (TD-C76K) via 8-bit

bus driver (IC2) to the Capstan Motor Drive Amplifier, the Switching Stabilizer, and the Spooling Motor Controller. One of three frequencies for clock signal TD-C307K can be selected (after having been buffered by IC2) with a jumper (JS7, JS8, and JS9).
To minimize power consumption, system clock E is also applied to the OE inputs (output enable) of the ROM and RAM (IC8, IC15, IC16, and IC18).
IC12 blocks the RAMSL signal when the reset signal is available in order to prevent access to the RAM during the reset phase. With IC4 and IC6 the R/W signal is logically combined with system clock E for correct timing during read/write access.
IC14 monitors the 5 V supply and produces a defined reset pulse during power on as well after transient power failures in operation. The system can be reset manually with key S1. With the TD-RESET signal the Tape Deck Serial Interface can also trigger a reset on the MPU. For this purpose the signal is ORed with button S1 through two resistors R6 and R7. The TD-RESET signal is active low and via R6 pulls pin2 of IC14 to low potential. Jumpers JS12...JS17 define the operating mode of MPU IC17. These jumper settings are fixed.
The address decoder IC11 (two 2-bit binary decoders) produces chip select signals from addresses A13, A14, and A15 for the ROMs, the RAM, and also produces an enable signal for IC3. IC3 is a bidirectional data bus buffer, the direction of which is determined by the read/ write signal R/W. An additional address decoder IC5 (3-bit binary decoder) produces select signals TD-SL2...-SL7, depending on addresses A10...A15. Select signals TD-SL2...5 are used for the interface assemblies which are addressed by means of memory mapping. The control bus is buffered by an 8-bit bus driver (IC1). IC2 buffers the address signal and clock signals as well as the reset (TD-RESMP) for the Tape Deck Serial IF.

3.2.6.2.2 **Tape Deck Serial Interface 1.820.763**

Functions:

- Serial communication between MP Unit Master and MP Unit Tape Deck Control.
- Analog/digital conversion of the output signals of the Tape Tension Sensors and the Spooling Motor Drive Amplifiers (motor current).

Circuit Description:

The serial TTL bus (TDS-RX, TDS-TX, TDS-DTR, TDS-CTS) from/to the Master Serial Interface is buffered by the 8-bit bus driver IC1 and connected to IC6, an SSDA (synchronous serial data adapter). Serial/parallel conversion (receive) or parallel/serial conversion (send) is performed synchronously by IC6. For this purpose Master Serial Interface supplies send/receive clock TDS-CLK, which is buffered by IC1. When a byte is received, IC6 triggers an IRQ (TD-IRQ) via IC12 at the processor of the MP Unit Tape Deck Control.
An 8-bit bus transceiver (IC2) buffers the data bus in both directions that leads from IC6/IC7 to the MP Unit Tape Deck Control.
A special address decoder has been implemented with IC8, a quad 2-to-1 data selector with inverting outputs. The switching direction (A or B to Y) is determined by the level of address TD-ADR3. The Y outputs are activated by signal TD-SL5 which is the select signal of this assembly. In this way IC2 receives an enable signal from IC8 only when the Tape Deck Serial Interface is selected by signal TD-SL5. In all other cases IC2 has high impedance on the output side, and the data bus of the MP Unit Tape Deck Control is in the correct state.
The analog voltage of the left and right tape tension sensors (AN-TTL and AN-TTR) are converted by analog/digital converter IC7. The analog signals AN-ICL and AN-ICR (voltage proportional to the actual spooling motor current) also need to be digitized. Because the actual voltage ranges from -5 V...+5 V, these voltages must first be transformed to the range required by IC7 (0...+5 V) by means of IC3. IC4 and IC5 are also designed for such level conversion, however, they are not required in this application (spare). Two retriggerable monoflops (IC11) are retriggered in regular intervals by the start signal for IC7. Should this retriggering fail, a reset (TD- RESET) is initiated by the MP Unit Tape Deck Control and the peripheral equipment is reset at the

same time by TD-RES. The TD-RESMP signal is output by MP Unit Tape Deck Control based on a power on reset or manual resetting with S1, and it is NORed by a gate of IC10 in order to reset peripheral equipment.

3.2.6.2.3 **Tape Deck Periphery Controller 1.820.762**

Functions:

- Controlling brake solenoids and two tape lifter controls.
- Reading sensor signals.

Circuit Description:

Two PIOs (parallel input/output) IC1 and IC2 are connected to the data bus, address bus, and control bus of MP Unit Tape Deck Control and consequently for direct access of the MPU.

The following signals are read in through port A (PA0...PA7) of the first PIO (IC1):

TAPE LIFTER POSITION SENSOR, left:	TD-RALP1, TD-RALP2
TAPE LIFTER POSITION SENSOR, right:	TD-RARP1, TD-RARP2
TRANSPARENT LEADER SENSOR:	TD-TRSP
SUPPLY VOLTAGE ON:	TD-SUPVON

Signals T-IRES1 and TD-SHLD are not used.

Port B of the PIO (IC1) is an 8-bit output. Following buffering with IC12, the enable signal for the Spooling Motor Control (TD-PENBL, TD- PENBR), the enable signal of the Spooling Motor Power Supply (TD-PWENB), and reset (TD-CRES) are output to the Capstan Control Unit.
The tape transport assembly is controlled with PB0...PB3. Timer chip IC10 is wired as a free-running oscillator with a frequency of approx. 240 Hz. IC9 (two-way JK flip-flop) produces two square-wave signals with a frequency of 60 Hz and 90° phase shift. IC and IC6 (quad NAND each) constitute an electronic changeover switch that is controlled by PB0 or PB1 respectively via D-register (IC5). As a result either output Q2 or the inverted output Q2 is connected to one NOR gate (IC8) each. PB2 and PB3 are connected to one NOR gate (IC8) each after being delayed by three D-registers. The transfer signal for octo D-register (IC5) is supplied by the inverted Q2 output of IC9. Buffer IC11 transfers the gated signals to the two Tape Lifter Controls.
Port PB of PIO (IC2) controls the brake solenoids. The level is matched by IC13, IC14, and IC15 (dual OR drivers).
Two comparators (IC3) digitize +YSUP signal which is read in via PA0 and PA1. PA2...PA7 are not used.

3.2.6.2.4 **Tape Lifter Control 1.820.773**

Tape lifter motor assembly (left)	1.820.140 GRP46
Tape lifter motor assembly (right)	1.820.141 GRP47

Functions:

- Transmission of the current position of the pinch roller assembly (2 bits per unit) to the Tape Deck Periphery Controller 1.820.762 (GRP20/ELM43).
- Control of the motor as specified by the Tape Deck Periphery Controller.

Circuit Description:

(This description relates to the left-hand motor, signal names for the right-hand motor are indicated in braces []).

- The position of the pinch roller assembly is determined by two forked IR light barriers in one housing (DLQ1) between which a specially designed shutter moves. The output signals of the light barriers are converted by IC1 (dual differential line receiver with Schmitt trigger characteristic) to TTL signals: TD-RALP1/TD-RALP2

[TD-RARP1/ TD-RARP2] and transmitted to the Tape Deck Periphery Controller (GRP20/ELM43).

- Motor control: A 3-phase delta-connected synchronous motor is used. Terminals b and c are connected to ground, terminals a and f as well as d and e are connected to two switching output stages (Q8, 9, and Q10, 11 respectively). These switch between + and -26 V with a frequency of 60 Hz. The phase shift of + or -90° between control signals TR-RALC1 and TD-RALC2 [TD-RARC1, TD-RARC2] determine the sense of the motor rotation. The motor moves the assembly out, when the TD-RALC2 signal leads relative to TD-RALC1 [TD-RALC2, TD RALC1]. When enable signal TD-RALEN [TD-RAREN] changes to high, the switching output stages are blocked and the motor stops. The two control signals TD-RACL2 and TD-RALC1 [TD-RARC2 and TD-RARC1] as well as enable signal TD-RALEN [TD-RAREN] are supplied by the Tape Deck Periphery Controller 1.820.762 (GRP20/ELM43).

3.2.6.2.5 **Opto Sensor PCB 1.820.793**

Function:

- Checks whether or not a tape is threaded and supplies a message to the Tape Deck Periphery Controller 1.820.762 (GRP20/ELM43) by means of TTL signal TD-TRSP.

Circuit Description:

The sensor consists of a double light barrier implemented with two phototransistors in one housing (QP1) and two LEDs (DL1, infrared / DL2, red). In the absence of tape the two phototransistors are supplied with light not only by the two light sources but also by ambient light; no current flows from the node between the two transistors to the inverting input of opamp IC3/pin 2 (manufacturing tolerances are compensated with R28). When tape is present, the upper phototransistor is dark, its impedance changes to high, and the current equilibrium is upset, i.e. a differential current flows to the input of opamp (IC3/pin 2). The output pin 3 of IC3 changes to positive (gain adjustable with R26). The Schmitt trigger IC2/1 (comparator with open-collector output) buffers the output signal of IC3/1 and pulls it to TTL level. It is transmitted as TD-TRSP signal to the Tape Deck Periphery Controller 1.820.762 (GRP20/ELM43).

Adjustments and test points: refer to par. 3.5.

3.2.6.2.6 **Tape Deck Counter/Timer 1.820.761**

Functions:

- Evaluation of the output signals from the spooling motor tacho boards and the Move Sensor.
- Supporting MPU Tape Deck Control regarding computations by means of a programmable timer.

Circuit Description:

The MP Unit Tape Deck Control has direct access to this unit via data bus, address bus, and control bus. The two signals TD-MOVE1 and TD- MOVE2 originate from the dual forked light barrier in the MOVE SENSOR. These are two square-wave TTL signals with a phase shift of 90° which are buffered with IC1 (six inverting Schmitt triggers) and are taken to one D-register (IC5) each. Transfer to output 8Q/7Q is effected with the positive edge of the processor clock (TD-ENB). IC5 and IC6 (4 EXORs) constitute a four-edge evaluator. The transfer value of TD-MOVE2 (7Q) is shifted through via 6D, 6Q, 5D to the output 5Q by means of two clock pulses. Via an EXOR it is gated with the actual level of TD-MOVE1 and taken as data signal to IC12 (D-flip-flop). The data signal identifies the running direction (H = forward, L = reverse). The D-flip- flop IC12 together with two NAND gates (IC11) constitutes an electronic change-over switch for the 8-bit up/down counter (IC19 and IC18). The input signals TD-MOVE1 and TD-MOVE2 are also EXORed and shifted through via 4D to 1Q by means of four clock pulses or to 2Q by three clock pulses. The logical combination with a second EXOR produces counting

pulses (TD-MVCLK) which are now transferred via two NAND gates (IC11) to the up/down counter and after inversion with IC7 to the synchronizer port. The TD-MVCLK signal is a pulse with a duration of 0.8 us and is delayed relative to the direction signal (TD-MVDIR) by an additional 0.8 us. Only when 4D and 4Q (IC5) have different levels is the NAND gate (IC11) enabled for connecting the processor clock (TD- ENB). This is necessary for the data signal to be accepted by IC12. The 8-bit counting value of IC19 and IC18 is connected by IC17 (8-bit bus driver) to the 8-bit bus transceiver when an enable is available from the address decoder IC15. This counter value is read by the MP Unit Tape Deck Control which computes the actual value from it.
The signals of the two spooling motor tachos are also processed by a four-edge evaluator (IC2, IC3, IC4, IC9, IC10). However, a programmable counter/timer (IC14) is used. The sense of rotation is transferred to IC16 via two D-flip-flops (IC10). The MPU thus reads the sense of rotation of the two spooling motors and the tape counter via IC16. The counter value for the spooling motors is read out of IC14.
IC8, a dual OR driver, retransmits the interrupt of IC14 to the MPU.

3.2.6.2.7 **Move Sensor PCB 1.820.770**

Function:

- Scanning and transmitting of the speed and rotation direction of the tape move sensor to the Tape Deck Counter/Timer 1.820.761 (GRP20/ELM44) in the form of two square-wave TTL signals with 90° phase shift.

Circuit Description:
The optical coding disc is rigidly connected to the move roller (idler roller at the tape scissors). The coding disc rotates between a dual, forked light barrier DLQ1. The output signals of the light barrier are converted to TTL signals by IC1 (dual differential line receiver with Schmitt trigger characteristic). Two trimmer potentiometers R2 and R9 are used for adjusting the duty cycle to 50%. The output signals of IC1 are buffered by IC2 (hex schmitt triggers) and transmitted to the Tape Deck Counter/Timer 1.820.761 (GRP20/ELM44); (signals TD-MOVE1, TD- MOVE2).

Adjustments: refer to par. 3.5

3.2.6.3 **Motor Control**

3.2.6.3.1 **Motor Tacho PCB 1.820.771 left and right**

Function:

- Scanning and transmitting of the speed and rotation direction of the spooling motor to the Tape Deck Counter/ Timer 1.820.761 (GRP20/ELM44) in the form of two square-wave TTL signals with 90° phase shift.

Circuit Description:
The optical coding disc is rigidly connected to the motor shaft. It rotates between a forked light barrier DLQ1. The output signals of the light barrier are converted to TTL signals by IC2 (dual differential line receiver with Schmitt trigger characteristic). Two trimmer potentiometers R11 and R12 are used for adjusting the duty cycle to 50%. The output signals of IC2 are buffered by IC1 (hex schmitt triggers) and transmitted to the Tape Deck Counter/Timer 1.820.761 (GRP20/ELM44); (left: TD-TML1/TD-TML-2; right: TD-TMR1/TD-TMR2).

Adjustments: refer to par. 3.5

3.2.6.3.2

Spooling Motor Controller PCB 1.820.760

Function:

- Based on the settings of the MPU Tape Deck Control (1.820.785; GRP20/ELM46), the Spooling Motor Controller produces analog output signals of the tape tension sensors (1.820.772, GRP42/43) as well as analog control signals for the Spooling Motor Driver (1.820.759, GRP20/ELM40) and that for each operating mode of the tape transport (STOP, PLAY, spooling, EDIT, SHUTTLE, TAPE DUMP, etc.).

Basically the following applies:

- The tape tensions of the supply and take-up reels are controlled when the tape speed is predetermined by the capstan motor (e.g. PLAY, REV PLAY);
- The back tension is controlled only when the pinch roller is released (e.g. ◄, ►, EDIT, SHUTTLE). The torque of the take-up motor is also controlled. The reference value in this case is not the tape tension but the spooling speed of the tape.
- The tape tension control loops are also enabled in STOP mode. The correcting variables (difference between desired and actual tape tension) of the left-hand and right-hand reel are effective on both sides so that the tape can be shuttled in either direction by manually turning one of the reels.

Circuit Description:

Parallel interface IC2 receives tape tension reference values from the MPU Tape Deck Control (1.820.785; GRP20/ELM46) via tape deck TTL bus and transmits these values to one of 6 multiplying D/A converter chips IC5, 8, 11, 13, 16, 17. Port A of IC2 transmits 8 data bits; the individual D/A converters are addressed via port B. The D/A converters fulfill different functions:

- Tape tension reference values are produced by IC5 (left) and IC 13 (right); IC4 pins 5,6,7 and IC12, pins 5,6,7 are responsible for converting output currents from IC5 and IC13 respectively into voltages; comparison between the actual value and the reference value is performed by IC4, pins 1,2,3 and IC12, pins 1,2,3.
- IC11 and IC17 multiply the difference between the reference value and the actual tape tension by a weighing factor that can vary depending on the tape transport mode and which takes into consideration the diameter of the reel and the corresponding pancake size. The output currents of IC11 and IC17 respectively are converted to voltages by IC6, pins 1,2,3 and IC14, pins 1,2,3.
- IC8 and IC7, pins 5,6,7 or IC17 and IC15, pins 5,6,7 produce a control voltage for the Spooling Motor Driver so that the controlling error can be minimized. This requires small corrections which in turn leads to greater system dynamics of the closed loop.

- PLAY mode:
  Tape speed is determined by the capstan motor, both spooling motors control tape tension. Active are: IC5 and IC13 for the reference value as well as IC11 and IC17 for multiplying the correcting variable (difference between desired and actual tape tension) by the weighing factor. IC8 and IC16 supply the expected control component to the control signals AN-IRL and AN-IRR.
- Spooling mode "fast forward": (rewind functions analogously)
  The speed of the take-up motor is determined by the spooling motor control loop (set point defined by MPU Tape Deck Control via IC16); IC17 does not contribute to the control signal AN-IRR; the speed is measured by the spooling motor tacho and reported to the Tape Deck Control 1.820.785 (GRP20/ELM46) via the Tape Deck Counter/ Timer 1.820.761 (GRP20/ELM44); the MPU Tape Deck Control regulates the nominal motor current via IC16).
  The supply motor controls the back tension as described under "PLAY mode".
- STOP:
  The tape stands still. Both spooling motors control tape tension, analog switch IC9. As a consequence the right-hand motor takes up tape when tape tension is decreased on the left-hand side (e.g. by turning the left-hand reel in the supply direction).

- TAPE OUT (tape unthreaded):
  Neither spooling motor receives control signals because analog switch IC3 connects AN-IRL and AN-IRR signals to ground.

3.2.6.3.3 **Spooling Motor Driver PCB 1.820.759**

Functions:

- Producing a pulse-width-modulated square-wave signal with a frequency of 76 kHz (PWMPL-H1 and PWMPR-H1) for each spooling motor output stage (Spooling Motor Drive Amplifier 1.820.775, GRP30/33). The duty cycle of this signal depends on input signal AN-IRL or AN-IRR respectively which is supplied by the Spooling Motor Controller (1.820.760, GRP20/ELM44), as well as on signal AN-ICLD or AN-ICRD which is proportional to the motor current.
- Since isolating transformers are located in the signal path of the Spooling Motor Drive Amplifier, the duty cycle must not be greater than approx. 98% and no less than approx. 2%.

Circuit Description:

Input signals AN-IRL and AN-ICLD (AN-IRR and IC-ICRD respectively) are subtracted from each other and amplified (IC4, IC3). Input signal TD-C76K (clock frequency of MP Unit Tape Deck Control) is inverted (IC10) and applied to the input of an integrator which reshapes it into a symmetrical triangular signal. The triangular signal is compared with the output signals of IC3 by two high-speed comparators (IC7, IC8). The result is two square-wave TTL signals with variable duty cycle. From the inverted input signal TD-C76K, the NAND gates of IC10 and IC11 produce narrow pulses of identical frequency which are added to the output signal of the two comparators. Should the comparator outputs be continually low or high, their output signal is replaced by the aforementioned pulses. The minimum and the maximum pulse width are, therefore, adhered to. Transistors Q4 and Q5 bring the control pulse level to CMOS level; the inverters in IC6 buffer these pulses. The output signals PWMPL-H1 and PWMPR-H1 are taken to the input of the two Spooling Motor Drive Amplifiers 1.820.775 (GRP30/33). The reset generator TL7705 (IC1) monitors the ±15 V voltages and enables the reset outputs if the voltages drop too strongly or if the TD-PENBR signal (from Tape Deck Periphery Controller 1.820.762, GR20/ELM43) is set to high. In this case outputs RESET (pin 5), RESET (pin 6), and Q5 block both output signals PWMPL-H1 and PWMPR-H1.

3.2.6.3.4 **Spooling Motor Drive Amplifier PCB 1.820.775**

Functions:

- Controlling a DC spooling motor in either sense of rotation based on a pulse-width-modulated control signal (left: PWMPL-H1; right: PWMPR-H1) from Spooling Motor Driver 1.820.759 GRP20/ELM40). Supply voltage: approx. 30 V. Maximum supply current: approx. 6 A.

Circuit Description: (refers to the left-hand motor)

Misprint in block diagram page 5/111: T3 → T2; T2 → T1; T1 → L3; C13,14 → C16,17. The pulse-width-modulated signal PWMPL-H1 (from the Spooling Motor Driver 1.820.759, GRP20/ELM40) is buffered and inverted (IC1). The inverted and noninverted signals are taken to the driver stages Q3, 4, 7, 8 or Q1, 2, 5, 6 respectively) via an edge delay circuit with different delay for the positive and negative edges (R3, D1, C4, IC1 or R10 respectively, D2, C10, IC1). Two pulse transformers T2 and T1 provide electrical insulation between the driver stages and the output stages. A VMOS power transistor is controlled by each winding (by T2 → Q12 and Q9, by T1 → Q10 and Q11). These four transistors are arranged in a bridge circuit. The aforementioned edge delay circuit prevents that a branch of the bridge is enabled before the other is disabled. The spooling motor is connected to the bridge circuit via a low-pass filter (L3, C16,17) and the current-to-voltage converter (R13-42, IC2). The output signal of the current-to-

voltage converter (AN-ICLD, 312.5 mV = 1 A) is returned to the input of the Spooling Motor Driver 1.820.759 and serves as a negative feedback.

Test points: Refer to par. 3.5.

3.2.6.3.5 **Tape Tension Sensor PCB 1.820.772**

(Tape tension sensor assembly 1.820.150 <left>, tape tension sensor assembly 1.820.151 <right>

Function:

- Measuring the tape tension. The angle by which the sensor lever is deflected is converted to an analog voltage (AN-TTL and AN-TTR respectively) and transmitted to the Spooling Motor Controller 1.820.760 (GRP20/ELM47) as well as to the Tape Deck Serial Interface 1.820.763 (GRP20/ELM47).

Circuit Description:

The angle sensor is a noncontacting Hall effect potentiometer (part No. 1.820.153.00). The negative voltage on the "wiper" is buffered by IC1/1. IC1/2 is an inverting amplifier. Its offset can be adjusted with trimmer potentiometer R7, its gain with trimmer potentiometer R9.

3.2.6.3.6 **Capstan Control Unit 1.820.764**

Function:

- Autonomous control of the capstan motor

Circuit Description:

IC16 is an 8-bit NMOS processor type MC 6803-1. The control program comprises 16 K-bytes and is stored in ROM (IC17). IC15 is a CMOS RAM with a capacity of 2 K-bytes.
With 8-bit D-latch IC14, IC16 assigns addresses A0...A7 of the multiplexed data/address bus to the address bus. The system clock E (enable pulse) is generated internally by IC16 with quartz accuracy and, after inversion (IC11), is applied to the retriggerable monoflop (IC8). After a second inversion, the clock is output as TC-ENB to the capstan interface.
For correct timing the system clock E is also applied to the OE (output enable) input of ROM and RAM (IC17 and IC15).
IC18 monitors the 5 V supply and produces a defined reset pulse during power on as well after transient power failures in operation. With key S1 the Capstan Control Unit can be reset manually. With the TD-CRES signal the Tape Deck Periphery Controller can also trigger a reset on the MPU. Jumpers JS1...JS3 define the operating mode of MPU IC16. These jumper settings are fixed.
The address decoder IC12 (two 2-bit binary decoders) produces the chip select signals from addresses A13, A14, and A15 for the ROM, the RAM, and also produces the enable signal for IC3 and IC2, and signals TC-SL1...-SL4. IC3 is a bidirectional data bus buffer, the direction of which is determined by the read/write signal RW.
The control bus is buffered by an 8-bit bus driver (IC2).

3.2.6.3.7 **Capstan Interface 1.820.727**

Functions:

- BUS interface between MP Unit Tape Deck Control and Capstan Motor Control for communication between the two MPUs.
- Digital/analog conversion for controlling the Capstan Motor Drive Amplifier.
- Switchover and processing of signals from an internal or external varispeed control.

Circuit Description:

This assembly is connected to the data, address, and control buses of the MPU Tape Deck Control (signals with TD-...) and of the Capstan Control Unit (signals with TC-...).

With TD-SL7 the MP Unit Tape Deck Control selects the PIO chip IC6. An 8-bit bus transceiver IC2 performs the required bus separation and buffering. IC11 is selected by the Capstan Control Unit via TC-SL1. The communication of the two MPUs is performed in interrupt mode. For this purpose the interrupt is always triggered on the opposite PIO. The buffering is performed by IC12. Interrupts from IC11, IC14 and those that are triggered by the Capstan Control Unit (TC-EREF) itself are NORed (IC10) to a single IRQ. Scanning determines which unit has triggered the IRQ.
A NAND gate of IC5 combines two select signals TC-SL1 and TC-SL2 as a logical OR and supplies the enable signal to the 8-bit bus transceiver IC1.
8 bits are transferred to the DAC (IC17) via IC13 (8-bit D-register). The reference voltage for the DAC is set with IC16. The analog voltage (0...10 V) is supplied to the Capstan Motor Drive Amplifier (AN-CSPDC) via IC15.
The tacho signals TD-TCM1/TD-TCM2 produced by the Tacho Sensor PCB are two square-wave TTL signals with 90° phase shift. The rotational direction signals TC-TCDIR (for the synchronizer) and TC-CDIRI for the Capstan Control Unit are produced by D-flip-flop IC9.
The two tacho signals TD-TCM1 and TD-TCM2 and transformed by two AND/OR/INVERT gates with 2 x 2 inputs (IC4) to a signal with double the frequency (TC-TCMV, TC-TCMVI). The momentary speed is determined by the Capstan Control Unit with TC-TCMVI. By contrast TCMV is intended for a synchronizer.
The changeover between the internal or external varispeed control is performed with the TC-INEX signal. The two signals T-REFINT (from the internal) and T-REFEXT (from an external varispeed control) are buffered in IC14 and are logically combined with the TC-INEX signal to the TC-REF signal by the second AND/OR/INVERT gate in IC14. This output signal is processed in the Capstan Control Unit and is returned as TC-REFP. D-flip-flop IC9 divides the TC-REFP signal by two and supplies the result to programmable divider IC14. The MPU of the Capstan Control Unit can now determine the desired (setpoint) speed based on the selected nominal speed and the reference frequency from the varispeed control.

3.2.6.3.8 **Tacho Sensor Electronics PCB 1.021.695**

Functions:

- Producing the capstan motor tacho signals TD-TCM1 and TCM2 (90° phase-shifted square-wave signals with TTL level) and transmission of these via Capstan Motor Drive Amplifier 1.820.774 to the Capstan Interface 1.820.727
- Preparation of the output signals of the three Hall-effect sensors on the Hall Sensor PCB 1.021.697 (built into the capstan motor, not accessible for service purposes) and transmission of these signals to the Capstan Motor Drive Amplifier 1.820.774 (GRP39).

Circuit Description:

- The capstan motor tacho consists of two insulating plastic rings. The inner circumference of these has teeth made of conductive plastic. The externally serrated flywheel (90 teeth) is rigidly coupled to the capstan motor shaft. Each plastic ring is subdivided into 6 segments of 14 teeth each. The teeth within each segment are electrically interconnected. These six segments form two electrically interconnected groups in which each of the 3 segments is offset by 120°. These two groups of 3 segments with the serrated flywheel in between can be considered as a variable capacitor whose capacitance fluctuates when the flywheel rotates (refer to Fig. 3.1.6). The frequency of the capacitance variation is 90 times greater than the rotational frequency of the capstan shaft. The two rings are mutually offset by half a tooth which means that not only the speed but also the sense of rotation can be detected with these rings.

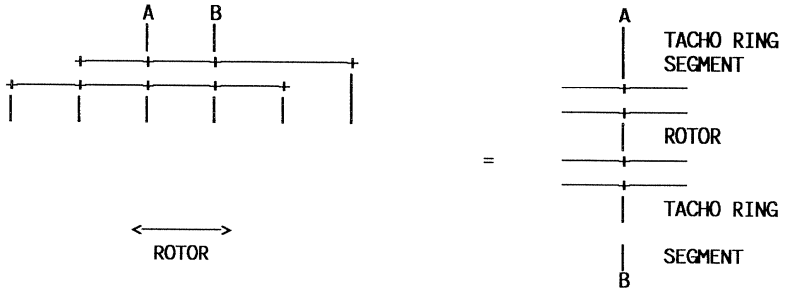


Fig. 3.1.6

The master oscillator (approx. 5.5 MHz) is implemented with Q1, L1 and C1. Its output signal is connected to the input of IC6 and IC7 (FM-IF amplifiers/demodulators). Together with the tuning coils L2 (of IC6) and L3 (of IC7), the variable capacitances inside the capstan motor form two parallel resonant circuits, which are also tuned to the frequency of the master oscillator. When the capstan motor turns, the tuning of the two parallel resonant circuits changes. The output of the two FM demodulators are AF signals of the same frequency as those of the capacitance change of the capstan motor tacho, with a phase shift of 90°. These two signals are first amplified by IC2/1 and IC5/1 respectively and subsequently converted to square-wave signals by the Schmitt triggers IC2/2 and IC5/2 respectively. The edge steepness is ultimately increased with two comparators (IC1). The open-collector outputs of the comparators (signals TD-TCM1 and TD-TCM2) are looped via the Capstan Motor Drive Amplifier 1.820.774 (GRP39) to the Capstan Interface 1.820.727 (GRP20/ELM42); the two pull-up resistors are also located there.

- The output signals of the three Hall effect sensors on the Hall Sensor PCB 1.021.697 are taken via the connector P2 to the Tacho Sensor Electronics PCB 1.021.695 (GRP38). The comparators IC3 and IC4/1 analyze the signals. The open-collector outputs of the comparators (signals TC-HALL1, TC-HALL2, and TC-HALL3) are connected to the inputs pin 10, 11 and 12 respectively of the Capstan Motor Drive Amplifier PCB 1.820.774 (GRP39); the three pull-up resistors are also located there.

3.2.6.3.9

Capstan Motor Drive Amplifier PCB 1.820.774

The capstan motor is a 3-phase motor with a multipole, permanent-field rotor, and a stator that is made up of 24 windings. Commutation is effected by Hall-effect sensors in the motor and by logical gating of the output signals from the Hall elements. The motor speed is determined solely by the operating voltage. The nominal operating voltage is 40 VDC.

Functions:

- Low-loss control of the motor speed via operating voltage by means of a switching voltage regulator (76 kHz) based on analog input signal AN-CSPDC from Capstan Interface 1.820.727 (GRP020/ELM42).
- Control of each of the three stator windings by means of a sine wave signal approximated by a three-stage (+, high impedance, ground) square-wave, as a function of output signals TC-HALL1...3 from the Tacho Sensor Electronics PCB 1.021.695 (GRP38) and the "rotation direction bit" TC-CAPDC from the Capstan Control Unit PCB 1.820.764 (GRP20/ELM41).

Circuit Description:

- The voltage regulator is implemented by IC4. It receives its clock frequency (TD-C76K, 76 kHz) from the MP Unit Tape Deck Control 1.820.785 (GRP20/ELM46). The clock frequency is monitored in the bandpass filter around IC6/2 and shaped into a square-wave signal by Schmitt trigger IC6/1 and subsequently with IC3 (one shot) to Dirac pulses of the same frequency. These pulses control the internal oscillator of IC4. If they fail, IC4 produces its own clock pulses. The reference value in the form of the signal AN-CSPDC (0 to 10 V) is produced by the Capstan Interface 1.820.727

(GRP20/ELM42), buffered by IC1/1, and compared by IC1/2 with the actual value. Voltage divider R14,38/R44 determines the factor by which the operating voltage of the motor is greater than AN-CSPDC (approx. 4). The correcting variable is taken via IC2/2 to the switching regulator chip IC4. The output of IC4 is connected to a high-speed switching stage with MOSFETs (Q1...8) which, together with L3 and C10, produces the capstan motor supply voltage (approx. 5...40 V, depending on the speed) from the +CAPMOT voltage.

- The 6 outputs of the logic control ICs, IC5, control one Darlington transistor each (Q10, Q12, Q14, Q16, Q18, Q20). Any two of these Darlington circuits can be regarded as a 3-position switch. Position 1: supply voltage; position 2: open; position 3: ground. These three switches produce the aforementioned sinusoidal signals C-PHASE-R, -S, and -T which are phase shifted by 120° each. The chronological order of the three phases is determined by signal TC-CAPDC; this means that also fast braking as well as reversing of the capstan motor is possible. The supply voltage of the logic control IC (IC5) is monitored by IC2/1. If it drops below approx. 4 V, correct functioning of IC5 is no longer ensured (the switching transistors might become damaged). For this reason the output of IC2/1 blocks the pulse width modulator; its output voltage drops to 0 V.

3.2.7 Troubleshooting and Servicing Aids

3.2.7.1 Internal Indicators

Check appropriate heading in par. 3.2

3.2.7.2 Testing with Terminal or PC

Described in Volo. III (servicing) of the D820X manuals and in par. 3.12

3.2.7.3 Adjusting the Analog Input Board 1.861.752/753

Factory adjustment only.

3.2.7.4 Adjusting the Analog Output Board 1.861.751

Factory adjustment only.

3.2.8 Options

3.3
List of Programmable IC's

List and crossreference of PAL and PROM version MK.0

Date of release of MK.0: 1987 / april 16

SW UPDATES:	1.861.853.22:	03.06.87
SW UPDATES:	1.861.854.21:	03.06.87
SW UPDATES:	1.861.861.21:	27.04.87
SW UPDATES:	1.861.861.22:	29.04.87
SW UPDATES:	1.861.860.21:	14.05.87
SW UPDATES:	1.861.742.22:	10.07.87
SW UPDATES:	1.861.818.22:	13.07.87
SW UPDATES:	1.861.816.23:	15.07.87
SW UPDATES:	1.861.862.24:	2.10.87
SW UPDATES:	1.861.853.23:	12.11.87
SW UPDATES:	1.861.860.22:	23.10.87
SW UPDATES:	1.861.803.21:	28.01.88
SW UPDATES:	1.862.862.71:	15.03.88 (SW INDEX 21)
SW UPDATES:	1.861.761.21:	04.05.88
SW UPDATES:	1.861.803.22:	08.06.88
SW UPDATES:	1.861.803.23:	08.06.88
SW UPDATES:	1.861.751.22:	10.06.88
SW UPDATES:	1.861.820.23:	20.06.88
SW UPDATES:	1.861.763.23:	20.06.88
SW UPDATES:	1.861.859.21:	15.09.88
SW UPDATES:	1.861.761.22:	21.09.88
SW UPDATES:	1.861.862.73:	22.11.88 (SW INDEX 23)
SW UPDATES:	1.861.817.21:	10.02.89
SW UPDATES:	1.861.763.24:	28.03.89 (10/89)
SW UPDATES:	1.861.820.24:	28.03.89 (10/89)
SW UPDATES:	1.861.742.23:	28.03.89 (10/89)
SW UPDATES:	1.861.764.20:	28.03.89 (10/89)
SW UPDATES:	1.861.764.21:	26.04.89 (12/89)
SW UPDATES:	1.861.820.25:	26.04.89 (12/89)
ADDED:	1.861.997.20:	15.07.87
ADDED:	1.861.761.20:	30.06.87
ADDED:	1.861.760.20:	27.07.87
ADDED:	1.861.764.20:	13.09.88
ADDED:	1.861.849.20:	09.05.89

A. PANELS

A1. DISPLAY PROCESSOR 1.861.742.20/22/23

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186140020	50140114	TBP28L22	1	DISADR	.ROM	.DOC	14
2	186140120	50140113	D2764-3	1	DISPAN	.ROM		3
2	186140123	50140113	D2764-3	1	DISPAN	.ROM		3
3	186140220	50180100	16V8	1	DP8BTRM	.GAL	(SYS)	12
3	186140222	50180100	16V8	1	DP8BTRMA	.GAL	(SYS)	12

A2. CCP TRANSCEIVER 1.861.744.20

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186140520	50180100	16V8	10	CCP8BREC	.GAL	(SYS)	2
2	186140620	50180100	16V8	10	CCP8BTRM	.GAL	(SYS)	5

A3. MP AMPLIFIER 1.861.746.20

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186141020	50180100	16V8	10	MCRECTRM	.GAL	(SYS)	4

B. HEAD- & CAGEELECTRONICS

B1. DETECTOR 1.861.804.20

DETECTOR II 1.862.809.20

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186141520	50180100	16V8	10	DETSYS	.GAL	(SYS)	29

B2. WRITE AMPLIFIER 1.861.803.20/21/22/23

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186142020	50180012	16-R8-A2CN	8	CHOPSEL	.PAL	TEST/TMG	0003
1	186142021	50180100	16V8	8	CHOPSELA	.GAL	TEST/TMG	0003
1	186142022	50180100	16V8	8	CHOPSELC	.GAL	TEST/TMG	0003
2	186142120	50180012	16-R8-A2CN	8	DEMUX3	.PAL	DATAMUX	0004
2	186142122	50180100	16V8	8	DEMUX4	.GAL	DATAMUX	0004
3	186142220	50180009	16-L8-A2CN	8	CHOPP2	.PAL	ENCHOPP	0007
3	186142223	50180100	16V8	8	CHOPP3	.GAL	ENCHOPP	0007
4	186142323	50180100	16V8	8	LATCH	.GAL	INIT.	0027

C. RACKELECTRONICS

C1. PDM MODULATOR 1.861.811.20

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186142520							

C2. PDM CONTROL 1.861.813.20

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186142620	50180100	16V8	1	PDM8BTRM	.GAL	(SYS)	10
2	186142720	50180100	16V8	1	PDM8BREC	.GAL	(SYS)	8

C3. CUE/PQ DELAY 1.861.816.20/23

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186142920	50140114	TBP28L22N	1	PDMTIME	.ROM	RAM-TMG	18
2	186194323	50160100	16V8	1	CUECNT	.GAL	DELAYADJ	12
3	186194323	50160100	16V8	1	CUECNT	.GAL	DELAYADJ	14

C4. DISPLAY INTERFACE 1.861.817.20/21

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186143020	50140114	TBP-28L-22		DISIF	.ROM	ADDR DEC	5
1	186143021	50140114	TBP-28L-22		DISIFA	.ROM	ADDR DEC	5

C5. MP Unit MASTER 1.861.818.20/22, 1.861.820.20/23/24

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186195020	50140125	HN4827128G		GILB4000	.ROM	MASTERSW	15
1	186195022	50140125	HN4827128G		GILB4000	.ROM	MASTERSW	15
1	186195023	50140125	HN4827128G		GILB4000	.ROM	MASTERSW	15
1	186195024	50140125	HN4827128G		GILB4000	.ROM	MASTERSW	15
1	186195025	50140125	HN4827128G		GILB4000	.ROM	MASTERSW	15
2	xxxxxxx20	50140125	HN4827128G		GILB8000	.ROM	MASTERSW	16
2	xxxxxxx22	50140125	HN4827128G		GILB8000	.ROM	MASTERSW	16
2	xxxxxxx23	50140125	HN4827128G		GILB8000	.ROM	MASTERSW	16
2	xxxxxxx24	50140125	HN4827128G		GILB8000	.ROM	MASTERSW	16
2	xxxxxxx25	50140125	HN4827128G		GILB8000	.ROM	MASTERSW	16
3	xxxxxxx20	50140125	HN4827128G		GILBC000	.ROM	MASTERSW	18
3	xxxxxxx22	50140125	HN4827128G		GILBC000	.ROM	MASTERSW	18
3	xxxxxxx23	50140125	HN4827128G		GILBC000	.ROM	MASTERSW	18
3	xxxxxxx24	50140125	HN4827128G		GILBC000	.ROM	MASTERSW	18
3	xxxxxxx25	50140125	HN4827128G		GILBC000	.ROM	MASTERSW	18
4	xxxxxxx22	50140125	HN4827128G		GILB2000	.ROM	MASTERSW	14
4	xxxxxxx23	50140125	HN4827128G		GILB2000	.ROM	MASTERSW	14
4	xxxxxxx24	50140125	HN4827128G		GILB2000	.ROM	MASTERSW	14
4	xxxxxxx25	50140125	HN4827128G		GILB2000	.ROM	MASTERSW	14
5	186195122	50180100	16V8		ADRSEL	.GAL	ADDSELEC	8
6	186195222	50180100	16V8		SIGSEL	.GAL	LOGICREP	10

D. BOX ELECTRONICS

D1. ANALOG OUTPUT 1.861.751.20

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186143320	50180100	16V8	2	SRMSB	.GAL	SHIFT-R	204
2	186143420	50180100	16V8	2	SRLSB	.GAL	SHIFT-R	205
3	186143520	50180100	16V8	2	COUNTER	.GAL	7B-CNTR	106
4	186143620	50180100	16V8	2	SRLSB	.GAL	SHIFT-R	105
5	186143720	50180100	16V8	2	SRMSB	.GAL	SHIFT-R	104
6	186143820	50140114	TBP-28L-22	2	TIMING	.ROM	TMG	107
7	186143920	50180100	16V8	2	DAREC	.GAL	(SYS)	140
7	186143922	50633000	16V8(SMD)	2	DAREC	.GAL	(SYS)	140
	186145320	50050206	82S-123N	2	FREDOUT1	.ROM	DACCORR	118
	186145420	50050206	82S-123N	2	FREDOUT2	.ROM	DACCORR	218

SET NUMBER FOR MATCHED DAC AND PROM COMBINATION:

	186149920	50050206	)					
		50190103	)MATCHED		DACCORR			

D2. ANALOG INPUT 1.861.752.20/1.861.753.20

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186144120	50180101	20V8	2	INTER	.GAL	2s COMP	5
2	186144220	50180100	16V8	2	MSAR-A	.GAL	SAR	10
3	186144320	50180100	16V8	2	MSAR-AB	.GAL	SAR	11
4	186144420	50180100	16V8	2	MSAR-B	.GAL	SAR	12
5	186144520	50180100	16V8	2	ADDRAM	.GAL	ADDER	8
6	186144620	50180012	16-R8A-2CN	2	FLGEN	.PAL	FLAG-GEN	4
7	186144720	50180100	16V8	2	MASTER	.GAL	6B-CNTR	2
8	186144820	50180017	16-C1-2CN	2	MMX	.PAL	P/S	16
9	186144820	50180017	16-C1-2CN	2	MMX	.PAL	P/S	17
10	186144920	50140114	TBP-28L-22	2	SAR	.ROM	TMG	3
11	186145020	50180100	16V8	2	ADREC	.GAL	(SYS)	20
12	186145120	50180010	16-R4A-2CN	2	CLP	.PAL	CLIPPING	25
	186144020	50050206	82S-123N	2	FREDIN1	.ROM	DACCORR	117
	186145220	50050206	82S-123N	2	FREDIN2	.ROM	DACCORR	217

SET NUMBER FOR MATCHED DAC AND PROM COMBINATION:

	186149920	50050206	)					
		50190103	)MATCHED		DACCORR			

D3. SYSTEM CONTROLLER 1.861.763.20/23/24

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186194120	50180100	16V8	10	MPUSBINT	.GAL	(SYS)	16
2	186194220	50140113	2764	10	SYSCON1	.ROM	EPROM	26
2	186194223	50140113	2764	10	SYSCON1	.ROM	EPROM	26
2	186194224	50140113	2764	10	SYSCON1	.ROM	EPROM	26
3	xxxxxxxxx	50140113	2764	10	SYSCON2	.ROM	EPROM	25
3	xxxxxxx23	50140113	2764	10	SYSCON2	.ROM	EPROM	25
3	xxxxxxx24	50140113	2764	10	SYSCON2	.ROM	EPROM	25
4	xxxxxxxxx	50140113	2764	10	SYSCON3	.ROM	EPROM	19
4	xxxxxxx23	50140113	2764	10	SYSCON3	.ROM	EPROM	19
4	xxxxxxx24	50140113	2764	10	SYSCON3	.ROM	EPROM	19
5	xxxxxxxxx	50140113	2764	10	SYSCON4	.ROM	EPROM	14
5	xxxxxxx23	50140113	2764	10	SYSCON4	.ROM	EPROM	14
5	xxxxxxx24	50140113	2764	10	SYSCON4	.ROM	EPROM	14

D3. EXTENDED SYSCON 1.861.764.20/21

REMARK TO RELEASE -20: WORKS WITH 1.861.820.24. NO EXTERNAL DP. NO MASTERING FUNCTION. NO SH RT FUNCTION. RELEASE -20 IS AN EMERGENCY VERSION TO BE USED ONLY IF -21 FAILS FOR SOME REASON. DATES: -20: 10/89; -21: 12/89.

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186194620	50180100	16V8	10	MPUSBIN2	.GAL	(SYS)	16
2	186194720	50180101	20V8	10	SYSADR	.GAL	DECODER	17
3	186194820	50140125	27128	10	EXTSYSC1	.ROM	PRGM	26
3	186194821	50140125	27128	10	EXTSYSC1	.ROM	PRGM	26
4	186194820	50140125	27128	10	EXTSYSC2	.ROM	PRGM	25
4	186194821	50140125	27128	10	EXTSYSC2	.ROM	PRGM	25
5	186194821	50140125	27128	10	EXTSYSC3	.ROM	PRGM	19

D4. GAINS CONTROL 1.861.853.20/21/22/23

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186145520	50180012	16-R8A-2CN	3	GC1REC8	.PAL	(SYS)	110
2	186145620	50180012	16-R8A-2CN	3	GC1TRM8	.PAL	(SYS)	210
3	186145720	50180011	16-R6A-2CN	3	1ADRDEC	.PAL	ADDRDECO	112
4	186145820	50180012	16-R8A-2CN	3	1QUALITY	.PAL	DISQUAL	212
5	186145920	50140113	D-2764-3	3	PULLOVER	.ROM	LEVELCNT	406
6	186146020	50180012	16-R8A-2CN	3	1DISCLIP	.PAL	DISPCLIP	206
7	186146120	50180003	20-R8ACN	3	1MUXTMG	.PAL	AESOTMG	101
7	186146122	50180003	20-R8ACN	3	1MUXTMGA	.PAL	AESOTMG	101
8	186146220	50180011	16-R6A-2CN	3	1DMUXTMG	.PAL	AESITMG	312
9	186146320	50180012	16-R8A-2CN	3	1DIVIDER	.PAL	DIVIDER	605
10	186146420	50180009	16-L8A-2CN	3	1AESDET	.PAL	SYNCDET	412
10	186146423	50180100	16V8	3	SYNDETA	.GAL	SYNCDET	412
11	186147420	50180012	16-R8A-2CN	3	2LOCK1	.PAL	LOCKDET	609
12	186147420	50180002	16-R8A-CN	3	2DIV256	.PAL	DIVIDER	510
13	186194520	50180012	16-R8A-2CN	3	1ADCCLIP	.PAL	ADCLIPP	503

D5. DAPRO IF 1.861.854.20/21

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186146520	50180013	20-L10-CN	3	2MAININP	.PAL	INPT.SEL	201
2	186146620	50140114	TBP-28L22N	3	2AES-F	.ROM	PREAMBLE	202
3	186146620	50180012	16-R8A-2CN	3	2B	.PAL	DEMOD	206
4	186146620	50180012	16-R8A-2CN	3	2A	.PAL	EDGEDET	207
5	186146720	50140114	TBP-28L22N	3	2AES-C	.ROM	PREAMBLE	209
6	186146820	50180010	16-R4A-2CN	3	2SYNCDA	.PAL	TIMING	210
7	186146920	50180012	16-R8A-2CN	3	2CRC2	.PAL	CRCGEN	303
7	186146921	50180012	16-R8A-2CN	3	2CRC2A	.PAL	CRCGEN	303
8	186146920	50180009	16-L8A-2CN	3	2CRC1	.PAL	CRCGEN	305
8	186146921	50180009	16-L8A-2CN	3	2CRC1A	.PAL	CRCGEN	305
9	186147020	50180003	20-R8A-CN	3	2G	.PAL	MODULAT.	304
10	186147120	50140114	TBP28L22	3	2AES-D	.ROM	TIMING	309
11	186147220	50180010	16-R4A-2CN	3	2E	.PAL	PRESYNC	307
12	186147320	50180006	10-L8-CN	3	2RAMTMG	.PAL	TIMING	406
12	186147321	50180006	10-L8-CN	3	2RAMTMGA	.PAL	TIMING	406

D6. DATA PROCESSOR 1.861.855.20

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186147520	50180012	16-R8A-2CN	4	3ADC16R8	.PAL	INREGCLP	301
2	186147520	50180012	16-R8A-2CN	4	3ADC16R8	.PAL	INREGCLP	303
3	186147620	50180015	20-X8-CN	4	3ADC20X8	.PAL	INREGCLP	302
4	186147620	50180015	20-X8-CN	4	3ADC20X8	.PAL	INREGCLP	304
5	186147720	50180005	10-H8-CN	4	3CLIP1	.PAL	DIGCLIPP	403
6	186147720	50180005	10-H8-CN	4	3CLIP1	.PAL	DIGCLIPP	404
7	186147820	50180005	10-H8-CN	4	3CLIP2A	.PAL	DIGCLIPP	402
8	186147920	50180012	16-R8A-2CN	4	3CONT1	.PAL	TMGGEN	203
9	186148020	50180013	20-L10-CN	4	3CONT2	.PAL	TMGGEN	210
10	186148120	50180011	16-R6A-2CN	4	3MU116R6	.PAL	MUX	408
11	186148220	50180010	16-R4A-2CN	4	3MU216R4	.PAL	MUX	409
12	186148220	50180010	16-R4A-2CN	4	3MU216R4	.PAL	MUX	410
13	186148220	50180010	16-R4A-2CN	4	3MU216R4	.PAL	MUX	411
14	186148220	50180010	16-R4A-2CN	4	3MU216R4	.PAL	MUX	412
15	186148320	50180011	16-R6A-2CN	4	3MU216R6	.PAL	MUX	406
16	186148320	50180011	16-R6A-2CN	4	3MU216R6	.PAL	MUX	407
17	186148420	50180011	16-R6A-2CN	4	3SPLA	.PAL	FLAGGEN	101
18	186148420	50180011	16-R6A-2CN	4	3SPLB	.PAL	FLAGGEN	102
19	186148520	50180009	16-L8A-2CN	4	3TWIN	.PAL	ERRFLSEL	312
20	186148620	50140114	TBP-28-L22	4	3PROM4	.ROM	TMG	204
21	186148720	50140150	6381-2	4	3DP7	.ROM	PRGMREG	205
22	186148720	50140150	6381-2	4	3DP8	.ROM	PRGMREG	206
23	186148720	50140150	6381-2	4	3DP16	.ROM	PRGMREG	207
24	186148720	50140150	6381-2	4	3DP10	.ROM	PRGMREG	208
25	186148720	50140150	6381-2	4	3DP11	.ROM	PRGMREG	209
26	186148820	50140111	N-82-S-185	4	3COUNT6	.ROM	PRGMSEL	211
27	186148820	50140111	N-82-S-185	4	3COUNT6A	.ROM	PRGMSEL	212
28	186148820	50140111	N-82-S-185	4	3COUNT5	.ROM	PRGMSEL	311

D7. COEFFICIENT GENERATOR 1.861.856.20/21

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186149020	50180008	16-A4-CJ	4	4ALU1	.PAL	ALU	410
2	186149020	50180008	16-A4-CJ	4	4ALU1	.PAL	ALU	411
3	186149020	50180008	16-A4-CJ	4	4ALU1	.PAL	ALU	412
4	186149120	50180008	16-A4-CJ	4	4ALU2	.PAL	ALU	409
5	186149220	50180006	10-L8-CN	4	4DEC4CH	.PAL	DEMUX	307
6	186149320	50140150	6381-2JS	4	4CG12	.ROM	CONT/TMG	201
7	186149320	50140150	6381-2JS	4	4CG13	.ROM	CONT/TMG	202
8	186149320	50140150	6381-2JS	4	4CG14	.ROM	CONT/TMG	203
9	186149320	50140150	6381-2JS	4	4CG15	.ROM	CONT/TMG	204
10	186149320	50140150	6381-2JS	4	4CG9	.ROM	CONT/TMG	205
11	186149420	50050206	82S123N	4	4KONST1A	.ROM	COEFF	108
12	186149420	50050206	82S123N	4	4KONST1B	.ROM	COEFF	208
13	186149520	50140114	TBP28L22N	4	4MOD5	.ROM	CIRC.MEM	308

D8. CODEC CONTROL 1.861.857.20

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186160020	50140120	TBP28S42N	5	M1A	.ROM	ADDGENTG	102
2	186160020	50140120	TBP28S42N	5	M1B	.ROM	ADDGEN	202
3	186160020	50140120	TBP28S42N	5	M2A	.ROM	ADDGEN	302
4	186160020	50140120	TBP28S42N	5	M2B	.ROM	ADDGEN	402
5	186160020	50140120	TBP28S42N	5	CODE	.ROM	CODEGEN	203
6	186160520	50140120	TBP28S42N	5	CNTR	.ROM	TMGGEN	103
7	186160620	50180010	16-R4A-2CN	5	BLOCKERR	.PAL	BLERRSEL	107
8	186160720	50180009	16-L8A-2CN	5	ERRMASK	.PAL	ERRMASK	108
9	186160820	50180008	10-L8A-CN	5	ERRMODE	.PAL	MODEDEC	109
10	186160920	50180012	16-R8A-2CN	5	CCRECTRA	.PAL	(SYS)	112
11	186161020	50180010	16-R4A-2CN	5	TMG	.PAL	DECOUTCK	207
12	186161120	50180012	16-R8A-2CN	5	TLFPRINT	.PAL	SQ/TLFP	211
13	186161220	50180010	16-R4A-2CN	5	ADDCOM	.PAL	MUTEGEN	307
14	186161320	50180011	16-R6A-2CN	5	MUTETMG1	.PAL	MUTETMG	309
15	186161420	50180010	16-R4A-2CN	5	DISPMODE	.PAL	SQ/CRC	310
16	186161520	50180011	16-R6A-2CN	5	FSPASS	.PAL	SQ/CORR	311
17	186161620	50180009	16-L8A-2CN	5	ADDGEN	.PAL	ADDRGEN	405
18	186161720	50180010	16-R4A-2CN	5	SPLDETSM	.PAL	SPLICE	409
19	186161820	50180012	16-R8A-2CN	5	WT1DIR	.PAL	8T-STGEN	410
20	186161920	50180011	16-R6A-2CN	5	CERR	.PAL	TLDET	509
21	186162020	50180012	16-R8A-2CN	5	WT0DELSM	.PAL	8T-STGEN	510
22	186162120	50180011	16-R6A-2CN	5	FLAGGEN	.PAL	FLAGGEN	609
23	186162220	50180011	16-R6A-2CN	5	SPCNTLSM	.PAL	SPCNTL	610
24	186162320	50180016	12-L6-CN	5	SPLTMG1	.PAL	SPLTMG1	611
25	186162420	50180006	10-L8-CN	5	SPLTMG2T	.PAL	SPLTMG2	612

D9. CODEC MEMORY 1.861.858.20

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186163520	50180015	20-X8-CN	6	PARITALU	.PAL	PAR.ALU	409
2	186163520	50180015	20-X8-CN	6	PARITALU	.PAL	PAR.ALU	509
3	186163620	50180012	16-R8A-2CN	6	ALUCNTL	.PAL	TMG	308
4	186163720	50180010	16-R4A-2CN	6	WRCNTL	.PAL	TMG/ERST	307
5	186163820	50180011	16-R6A-2CN	6	ERRST	.PAL	ERRSTGEN	310
6	186163920	50180012	16-R8A-2CN	6	IOCNTL	.PAL	TMG	309
7	186164020	50180010	16-R4A-2CN	6	FLAGSEL	.PAL	FLAGSEL	111
8	186164120	50180006	10-L8-CN	6	RAMOE2	.PAL	DEMUX	305
9	186164220	50180006	10-L8-CN	6	RAMWR2	.PAL	DEMUX	306
10	186164320	50180011	16-R6A-2CN	6	ILVTMG	.PAL	SPLCNTL	311
11	186164320	50180012	16-R8A-2CN	6	ILVCNTR	.PAL	SPLDEILV	312
12	186164320	50180011	16-R6A-2CN	6	ILVMASK0	.PAL	IDISCORR	412
13	186164320	50180014	20-R4A-CN	6	ILVMASK1	.PAL	IINHIBIT	512

D10. TRANSFORMATTER 1.861.859.20/21

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186164520	50180010	16-R4A-2CN	7	FLAGSC	.PAL	FLAGSEL	210
1	186164521	50180100	16V8	7	FLAGSD	.GAL	FLAGSEL	210
2	186164620	50180100	16V8	7	FORMSB	.GAL	FORMATT	209
3	186164720	50180100	16V8	7	FORMA	.GAL	ADDRSEL	311
4	186164820	50180100	16V8	7	FORMB	.GAL	ADDRSEL	310
5	186164920	50180100	16V8	7	FORMC	.GAL	ADDRSEL	309
6	186165020	50180100	16V8	7	HDM3	.GAL	MODULATE	105
7	186165120	50180100	16V8	7	DATS3	.GAL	DATASEQ	107
8	186165220	50180100	16V8	7	SEQAD	.GAL	SEQ.ADDR	208
9	186165320	50180100	16V8	7	SPRED	.GAL	DATA.OUT	106
10	186165420	50180100	16V8	7	RACNT1	.GAL	REF.ADDR	409
11	186165520	50180100	16V8	7	RACNT2	.GAL	REF.ADDR	408
12	186165620	50180101	20V8	7	ADPR1A	.GAL	ADDRPROC	603
13	186165720	50180100	16V8	7	CSELT	.GAL	RAM.SEL	508
14	186165820	50180100	16V8	7	ADDCY	.GAL	ADDCARRY	503
15	186165920	50180100	16V8	7	TLOOP	.GAL	TESTLOOP	203
16	186166020	50180100	16V8	7	GUESL	.GAL	MISC.	404
17	186166120	50180100	16V8	7	SYDETE	.GAL	SYNCDET	202
18	186166220	50180100	16V8	7	SECNT2B	.GAL	RAMSECT.	302
19	186166320	50180100	16V8	7	SERVOB	.GAL	SCONTROL	101
20	186166420	50180100	16V8	7	ERRFLD	.GAL	ERRFLAG	510
21	186166620	50180100	16V8	7	BLNRB	.GAL	BLNOCNTR	501
22	186166720	50180100	16V8	7	BLSEQB	.GAL	BLOCKSEQ	602
23	186166820	50180100	16V8	7	RTSYC	.GAL	RTSYNC	401
24	186166920	50140151	AM27S29	7	FORM	.ROM	FORMADDR	411
25	186167020	50180100	16V8	7	ADPR2	.GAL	ADDRPROC	502
26	186167120	50180100	16V8	7	SPLDET	.GAL	SPLDET	601

D11. RUN PROCESSOR 1.861.860.20/21/22

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186167520	50180002	16-R8A-CN	8	EDET	.PAL	EDGEDET	509
2	186167520	50180002	16-R8A-CN	8	EDET	.PAL	EDGEDET	510
3	186167520	50180002	16-R8A-CN	8	EDET	.PAL	EDGEDET	511
4	186167520	50180002	16-R8A-CN	8	EDET	.PAL	EDGEDET	512
5	186167620	50180011	16-R6A-2CN	8	ABSEL	.PAL	A/B.SEL	508
6	186167720	50180003	20-R8A-CN	8	RAMCON	.PAL	CNTRADDR	204
7	186167820	50180002	16-R8A-CN	8	SUMOUT	.PAL	CNTRADDR	203
8	186167920	50140111	82S185N	8	A0X	.ROM	TAPETABL	401
9	xxxx679xx	50140111	82S185N	8	A1X	.ROM	TAPETABL	402
10	xxxx679xx	50140111	82S185N	8	A2X	.ROM	TAPETABL	403
11	xxxx679xx	50150111	82S185N	8	A3X	.ROM	TAPETABL	404
12	xxxx679xx	50140121	82S129	8	PREDIQ	.ROM	QUANTIZE	302
13	xxxx679xx	50140111	82S185N	8	A4X	.ROM	TAPETABL	503
14	xxxx679xx	50140111	82S185N	8	A5X	.ROM	TAPETABL	504
15	186168320	50180009	16-L8-A2CN	8	ROMSEL	.PAL	ROM.SEL	501
15	186168322	50180100	16V8	8	ROMSEL	.PAL	ROM.SEL	501
16	186168420	50180012	16-R8A-2CN	8	TRCOD	.PAL	TRANSCOD	308
17	186168520	50180011	16-R6A-2CN	8	FIFINT	.PAL	FIFO.IN	309
17	186168521	50180100	16V8	8	FIFINT	.PAL	FIFO.IN	309
18	186168620	50180011	16-R6A-2CN	8	FIFOUT	.PAL	FIFO.OUT	311
19	186168720	50180012	16-R8A-2CN	8	DECAT	.PAL	HDMDEMOD	312
20	186168820	50180012	16-R8A-2CN	8	DECOD	.PAL	HDMDEMOD	210
20	186168821	50180100	16V8	8	DECOD	.PAL	HDMDEMOD	210
21	186168920	50180011	16-R6A-2CN	8	DECOUT	.PAL	HDMDEMOD	211
21	186168921	50180100	16V8	8	DECOUT	.PAL	HDMDEMOD	211

D11. ADAPTIVE RUN PROCESSOR 1.861.760.20

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186167520	50180100	16-V-8	8	EDET	.GAL	EDGEDET	509
2	186167520	50180100	16-V-8	8	EDET	.GAL	EDGEDET	510
3	186167520	50180100	16-V-8	8	EDET	.GAL	EDGEDET	511
4	186167520	50180100	16-V-8	8	EDET	.GAL	EDGEDET	512
5	186167620	50180100	16-V-8	8	ABSEL	.GAL	A/B.SEL	508
6	186167720	50180101	20-V-8	8	RAMCON	.GAL	CONTROL	203
7	186167820	50180100	16-V-8	8	SUMOUT	.GAL	NIBBACCU	202
8	186167920	50142003	CY7C263-40C	8	TABAMP	.ROM	TAPETABL	402
9	186168020	50142003	CY7C263-40C	8	TABxxx	.ROM	TAPETABL	401
10	186169020	50180100	16-V-8	8	COMB	.GAL	RUNLIMIT	403
11	186169120	50180100	16-V-8	8	DEV	.GAL	DEVIAT.	404
12	186168120	50140121	82S129	8	PREDIQ	.ROM	QUANTIZE	302
13	186169220	50180100	16-V-8	8	LIM	.GAL	RUNLIMIT	405
14	186169320	50180100	16-V-8	8	VALD	.GAL	RUNLIMIT	406
15	186169420	50180100	16-V-8	8	CORRL	.GAL	CORLATCH	505
16	186168420	50180100	16-V-8	8	TRCOD	.GAL	TRANSCOD	308
17	186168520	50180100	16-V-8	8	FIFINTA	.GAL	FIFO.IN	309
18	186168620	50180100	16-V-8	8	FIFOUT	.GAL	FIFO.OUT	311
19	186168720	50180100	16-V-8	8	DECAT	.GAL	HDMDEMOD	312
20	186168820	50180100	16-V-8	8	DECOD	.GAL	HDMDEMOD	210
21	186168920	50180100	16-V-8	8	DECOUT	.GAL	HDMDEMOD	211
22	186169520	50180100	16-V-8	8	PAST	.GAL	PASTRUN	506
23	186169620	50180100	16-V-8	8	ECNT1	.GAL	EVENTS	501
24	186169720	50180100	16-V-8	8	ECNT2	.GAL	EVENTS	502
25	186169820	50180100	16-V-8	8	ECNT3	.GAL	EVENTS	503
26	186169920	50140150	CY7C281-45C	8	CORRT	.ROM	CORRTABL	504

ROM TAPETABLE TABxxx
FOR 1.861.760.20

xxx	TAPE A	xxx	TAPE B
AMP	AMPEX, SONY, 3M		

D12. RT/TC CODEC 1.861.861.20/21/22

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186190020	50180011	16-R6A-2CN	8	RAMST	.PAL	BIPH.MOD	201
2	186190120	50180011	16-R6A-2CN	8	ADMOD	.PAL	ADD.MOD.	202
2	186190121	50180011	16-R6A-2CN	8	ADMODI	.PAL	ADD.MOD.	202
3	186190220	50180011	16-R6A-2CN	8	CONSYN	.PAL	SYSSTART	203
4	186190320	50180012	16-R8A-2CN	8	CONSYS	.PAL	SYSBUS	204
5	186190420	50180011	16-R6A-2CN	8	AD1	.PAL	COUNTER	208
5	186190422	50180011	16-R6A-2CN	8	AD1A	.PAL	COUNTER	208
6	186190520	50180012	16-R8A-2CN	8	SYN	.PAL	INPTSYNC	209
6	186190522	50180012	16-R8A-2CN	8	SYNA	.PAL	INPTSYNC	209
7	186190620	50180012	16-R8A-2CN	8	WIND	.PAL	WINDOW	211
8	186190720	50180012	16-R8A-2CN	8	SING	.PAL	DETECTOR	212
8	186190722	50180012	16-R8A-2CN	8	SING2	.PAL	DETECTOR	212
9	186190820	50180012	16-R8A-2CN	8	RAMAD1	.PAL	ADDR.GEN	401
10	186190920	50180012	16-R8A-2CN	8	RAMAD2	.PAL	ADDR.GEN	402
11	186191020	50180011	16-R6A-2CN	8	RAMAD3	.PAL	ADDR.GEN	403
12	186191120	50180011	16-R6A-2CN	8	TIMING	.PAL	TMG.GEN.	404
13	186191220	50180011	16-R6A-2CN	8	SECAD	.PAL	SECT.ADR	405
14	186191320	50180011	16-R6A-2CN	8	CROWN	.PAL	CNTRDOWN	408
15	186191420	50180011	16-R6A-2CN	8	CUP	.PAL	CNTR-UP	409
15	186191422	50180011	16-R6A-2CN	8	CUP2	.PAL	CNTR-UP	409
16	186191520	50180015	20-X8-CN	8	SYSAD2	.PAL	SYSCON	410
17	186191620	50180015	20-X8-CN	8	SYSAD1	.PAL	RAMWRITE	411
17	186191622	50180015	20-X8-CN	8	SYSAD1A	.PAL	RAMWRITE	411
18	186191720	50180015	20-X8-CN	8	AD2	.PAL	RAMADDR	412
18	186191722	50180015	20-X8-CN	8	AD2A	.PAL	RAMADDR	412
19	186191820	50180012	16-R8A-2CN	8	SPEEDIS	.PAL	DISPLAY	505
20	186191920	50180012	16-R8A-2CN	8	SHIFT	.PAL	SHIFTREG	509
21	186192020	50180012	16-R8A-2CN	8	TCSYS	.PAL	ADDRDEC	510
22	186196120	50180009	16-L8A-2CN	8	DETECT	.PAL	SYSCON	511
22	186196122	50180009	16-L8A-2CN	8	DETECTA	.PAL	SYSCON	511
23	186196220	50180011	16-R6A-2CN	8	RD2	.PAL	RAMREAD	512
23	186196222	50180010	16-R4A-2CN	8	RD2A	.PAL	RAMREAD	512
24	186196320	50180012	16-R8A-2CN	8	CNTCL	.PAL	CLK.GEN.	601
25	186196420	50180010	16-R4A-2CN	8	ADSWI	.PAL	ADDR.SEL	602
26	186196520	50180011	16-R6A-2CN	8	SYSDEMA	.PAL	SYNC.DET	604
27	186196620	50180012	16-R8A-2CN	8	RTCL	.PAL	RUN CNTR	605
28	186196720	50180012	16-R8A-2CN	8	TCMOD	.PAL	MODULAT.	607
29	186196820	50180010	16-R4A-2CN	8	SYSTMG	.PAL	TMGGEN	608
29	186196822	50180010	16-R4A-2CN	8	SYSTMGA	.PAL	TMGGEN	608
30	186196920	50180010	16-R4A-2CN	8	MASTER	.PAL	CHIPCONT	609
30	186196922	50180010	16-R4A-2CN	8	MASTERA	.PAL	CHIPCONT	609
31	186197020	50180010	16-R4A-2CN	8	WR2	.PAL	RAMWRITE	610
31	186197022	50180011	16-R6A-2CN	8	WR2A	.PAL	RAMWRITE	610
32	186197120	50180011	16-R6A-2CN	8	RD1	.PAL	RAMREAD	611
32	186197122	50180011	16-R6A-2CN	8	RD1A	.PAL	RAMREAD	611
33	186197220	50180014	20-R4A-CN	8	OUT	.PAL	FRAMEINV	606
33	186197222	50180014	20-R4A-CN	8	OUTA	.PAL	FRAMEINV	606

D12. RT/TC CODEC II 1.861.761.20/21/22

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186190020	50180100	16-V-8	8	RAMST	.GAL	BIPH.MOD	201
2	186190120	50180100	16-V-8	8	ADMODI	.GAL	ADD.MOD.	202
3	186190220	50180100	16-V-8	8	CONSYN	.GAL	SYSSTART	203
4	186190320	50180100	16-V-8	8	CONSYS	.GAL	SYSBUS	204
5	186190420	50180100	16-V-8	8	AD1A	.GAL	COUNTER	208
6	186190520	50180100	16-V-8	8	SYNA	.GAL	INPTSYNC	209
7	186190620	50180012	16-R8A-2CN	8	WIND	.PAL	WINDOW	211
7	186190621	50180100	16-V-8 !!!	8	WINDA	.GAL	WINDOW	211
8	186190720	50180012	16-R8A-2CN	8	SING2	.PAL	DETECTOR	212
8	186190721	50180012	16-R8A-2CN	8	SING2A	.PAL	DETECTOR	212
8	186190722	50180100	16-V-8	8	SINGC	.GAL	DETECTOR	212
9	186190820	50180100	16-V-8	8	RAMAD1	.GAL	ADDR.GEN	401
10	186190920	50180012	16-R8A-2CN	8	RAMAD2	.PAL	ADDR.GEN	402
10	186190921	50180100	16-V-8 !!!	8	RAMAD2A	.GAL	ADDR.GEN	402
11	186191020	50180100	16-V-8	8	RAMAD3	.GAL	ADDR.GEN	403
12	186191120	50180100	16-V-8	8	TIMING	.GAL	TMG.GEN.	404
13	186191220	50180100	16-V-8	8	SECAD	.GAL	SECT.ADR	405
14	186191320	50180100	16-V-8	8	CROWN	.GAL	CNTRDOWN	408
15	186191420	50180100	16-V-8	8	CUP2	.GAL	CNTR-UP	409
16	186191520	50180015	20-X8-CN	8	SYSAD2	.PAL	SYSCON	410
17	186191620	50180015	20-X8-CN	8	SYSAD1A	.PAL	RAMWRITE	411
18	186191720	50180015	20-X8-CN	8	AD2A	.PAL	RAMADDR	412
19	186191820	50180100	16-V-8	8	SPEEDIS	.GAL	DISPLAY	505
20	186191920	50180012	16-R8A-2CN	8	SHIFT	.PAL	SHIFTREG	509
20	186191921	50180100	16-V-8	8	SHIFTA	.GAL	SHIFTREG	509
21	186192020	50180100	16-V-8	8	TCSYS	.GAL	ADDRDEC	510
22	186196120	50180100	16-V-8	8	DETECTA	.GAL	SYSCON	511
23	186196220	50180010	16-R4A-2CN	8	RD2A	.PAL	RAMREAD	512
23	186196221	50180010	16-R4A-2CN	8	RD2B	.PAL	RAMREAD	512
23	186196222	50180100	16-V-8	8	RD2C	.GAL	RAMREAD	512
24	186196320	50180012	16-R8A-2CN	8	CNTCL	.PAL	CLK.GEN.	601
24	186196321	50180100	16-V-8	8	CNTCLA	.GAL	CLK.GEN.	601
25	186196420	50180100	16-V-8	8	ADSWI	.GAL	ADDR.SEL	602
26	186196520	50180100	16-V-8	8	SYSDEMA	.GAL	SYNC.DET	604
27	186196620	50180100	16-V-8	8	RTCL	.GAL	RUN CNTR	605
28	186196720	50180012	16-R8A-2CN	8	TCMOD2	.PAL	MODULAT.	607
28	186196721	50180100	16-V-8	8	TCMODI	.GAL	MODULAT.	607
29	186196820	50180100	16-V-8	8	SYSTMGA	.GAL	TMGGEN	608
30	186196920	50180100	16-V-8	8	MASTERA	.GAL	CHIPCONT	609
31	186197020	50180011	16-R6A-2CN	8	WR2A	.PAL	RAMWRITE	610
31	186197021	50180011	16-R6A-2CN	8	WR2B	.PAL	RAMWRITE	610
31	186197022	50180100	16-V-8	8	WR2C	.GAL	RAMWRITE	610
32	186197120	50180011	16-R6A-2CN	8	RD1A	.PAL	RAMREAD	611
32	186197121	50180011	16-R6A-2CN	8	RD1B	.PAL	RAMREAD	611
32	186197122	50180100	16-V-8	8	RD1C	.GAL	RAMREAD	611
33	186197220	50180101	20-V-8	8	OUTA	.GAL	FRAMEINV	606
34	186197321	50180100	16-V-8	8	DEL	.GAL	RDY.CLR	504

D13. TIMING + TEST 1.861.862.20/24/71/73 (INDEX 23)

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186192120	50180100	16V8	9	TT8BREC	.GAL	(SYS)	206
2	186192220	50180100	16V8	9	INCKSEL	.GAL	INPT SEL	308
3	186192320	50180100	16V8	9	VASPH	.GAL	VARISPDH	309
4	186192420	50180100	16V8	9	VASPL	.GAL	VARISPDL	310
5	186192520	50180009	16-L8A-2CN	9	SYNDET	.PAL	SYNC DET	402
5	186192524	50180100	16V8	9	SYNDETA	.GAL	SYNC DET	402
6	186192620	50180100	16V8	9	DIV80M	.GAL	DIV 112	403
7	186192720	50180100	16V8	9	DIV5M	.GAL	DIV 189	404
8	186192820	50180010	16-R4A-2CN	9	DIV5	.PAL	DIV 5	405
8	186192821	50180100	16V8	9	DIV5Q	.GAL	DIV 5	405
9	186192920	50180010	16-R4A-2CN	9	PLLSEL	.PAL	INPT SEL	406
9	186192921	50180100	16V8	9	PLLSELA	.GAL	INPT SEL	406
10	186193020	50180100	16V8	9	DIV192	.GAL	DIV 192	507
11	186193120	50140114	TBP-28-L22	9	PRESYNC	.ROM	PRESYNC	508
11	186193123	50140114	TBP-28-L22	9	PRESYNCA	.ROM	PRESYNC	508
12	186193220	50140114	TBP-28-L22	9	VCXL1	.ROM	BYTE LOW	509
13	186193320	50140114	TBP-28-L22	9	VCXM1	.ROM	BYTE MID	510
14	186193420	50180100	16V8	9	VCXH2F	.GAL	BYTE HI	511
15	186193520	50180100	16V8	9	PRESYNC	.GAL	PRESYNC	607
15	186193523	50180100	16V8	9	TTLOCKA	.GAL	PRESYNC	607
16	186193620	50180100	16V8	9	DIV72	.GAL	DIV 72	702
17	186193720	50180100	16V8	9	DIV12	.GAL	DIV 12	703
18	186193820	50180100	16V8	9	RANGE	.GAL	RANGEDET	704
19	186193920	50180100	16V8	9	TT8BTRM	.GAL	(SYS)	705

D14. MASTERING INTERFACE 1.861.849.20

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186162620	50180100	16V8	0	RDADCNT	.GAL	RAMCONTR	10
2	186162720	50180100	16V8	0	WRADCNT	.GAL	RAMCONTR	11
3	186162820	50180100	16V8	0	AESREG	.GAL	DATASTOR	13
4	186162920	50180100	16V8	0	DEMAES	.GAL	DEMOD	14
5	186163020	50180100	16V8	0	PHCORR	.GAL	PHASECOR	20
4	186163120	50180100	16V8	0	MUTEC	.GAL	MUTECONT	21
5	186163220	50180100	16V8	0	OUTDAC	.GAL	FORMAT	22

E 1. CRC COUNTER 1.861.997.20

NO	DACA-NO.	STOCK-NO.	TYPE	REG	DESCR.	MEM	APPLIC.	POSNO
1	186194420	50180100	16-V-8		BURSTCNT	.GAL	COUNTER	21
1	186194420	50180100	16-V-8		BURSTCNT	.GAL	COUNTER	22
1	186194420	50180100	16-V-8		BURSTCNT	.GAL	COUNTER	23
1	186194420	50180100	16-V-8		BURSTCNT	.GAL	COUNTER	24
1	186194420	50180100	16-V-8		BURSTCNT	.GAL	COUNTER	25
1	186194420	50180100	16-V-8		BURSTCNT	.GAL	COUNTER	26
1	186194420	50180100	16-V-8		BURSTCNT	.GAL	COUNTER	27
1	186194420	50180100	16-V-8		BURSTCNT	.GAL	COUNTER	28

Abbreviations:
DACA = data carrier
PAL = programmable array logic (TM AMD)
GAL = generic array logic
ROM = read only memory (also PROM, EPROM)
SYS = system controller module
MEM = memory type
POSNO = position number
APPLIC. = application
DESCR. = description (DACA name)

Remarks:
ROM-SETS: top-no. denotes set-no.
numbers denoted with xxxxyyyxx are reserved

3.4
Servicing Displays on Boards

3.5 Service Adjustments

3.5.1 Equipment Required

- Digital Multimeter
- Oscilloscope
- Frequency counter
- Spring dynamometer 0 - 5 N (0 to 500 g) Part No. 10.249.001.01
- Spring dynamometer 0 - 20 N (0 to 2 kg) Part No. 10.249.001.03
- Gauge for adjusting the tape tension sensors Part No. 10.010.001.30
- Device for adjusting the tape tension springs incl. 2 weights Part No. 10.010.001.31
- Tentelometer 1/4" - 1" Part No. 10.300.001.01
- Extender board (see par. 1.5)
- Grease pen Part No. 10.401.001.01

3.5.2 Saturation Current Adjustment

Definitions for recording current settings as specified for the D820x in the final test dept. The settings specified are common practice within the DASH group of manufacturers.

3.5.2.1 Digital Tracks

The recorders are aligned at the final test department to the point of -0.2 dB below saturation recording current in order to obtain a more accurate reading than would be obtained if the operating point were adjusted to saturation flux. The range for saturation current may be very broad, especially with thin film recording heads. Measurement condition: frequency = 1/1.5 T (192 kHz). Select the jumper connectors on the write amplifier accordingly (see chapter 3.4.

3.5.2.2 Cue Tracks, Modulated

Recording current setting for cue tracks: see figure nnn.
The above defined point for optimal recording current setting yields high output and at the same time the lowest distortion for video grade tapes.
The permitted tolerance band for recording current setting is 0.5 dB, which is from the saturation recording current value to -0.5 dB from this value. Measurement condition: frequency = 1/1.5 T (192 kHz).

3.5.2.3 Time Code Track, Modulated

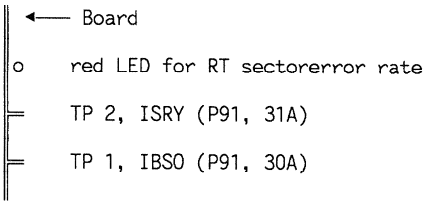
The tape flux is set for -0.25 dB below saturation recording current, which also yields optimum eye pattern performance.
The permitted tolerance band for recording current setting is 0.5 dB, which is from the saturation recording current value to -0.5 dB from this value.
Measurement frequency 1/T(tc) = 4 fs.
Refer to the figure given for cue tracks.

3.5.2.4 Reference Time Track

The identical record current setting as for the digital tracks is used and increased by 20 %, ±10 %.
In the D820X is the reference track adjusted together with the digital tracks and the above given condition is established automatically by the selection of the series resistors with the write head drivers on the write amplifier board.
The criteria here is to be able to overwrite a tape which has been recorded previously upside down. The D820X permits this mode at a slightly inferior blockerror rate.

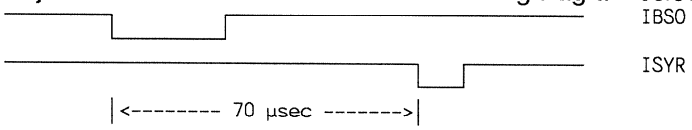
3.5.3
Head Distance

Board RT/TC Codec 1.861.761 contains two test pins located at the front of the board (opposite card connector).



Adjustment procedure:

- Adjust tape tension
- Connect probes of dual beam scope to test point 1 and 2
- Set recorder to RECORD mode with 48 kHz sampling frequency
- Adjust head distance as indicated in the timing diagram below:



The negative going leading edge of signal ISYR (from IC 101, pin 7) must follow the negative going leading edge of signal IBSO (IC 201, pin 9) with 70 µsec as closely as possible. Confirm adjustment by performing punch-ins and -outs on a prerecorded tape.
Head distance adjustment is necessary after head or headblock exchange and after exchange of the capstan motor.

3.5.4
Power Supply Tape Transport

Checking the supply voltages:

- Swing down amplifier bay.
- On FUSE/SUPPLY FAILURE DETECTOR PCB 1.820.737 measure the voltage to ground (TP3) on the following test points (from left to right):
- TP11: +5.6 V ± 0.1 V (adjustable with R21 on SWITCHING STABILIZER PCB 1.820.790)
- TP10: +24 V ± 1 V
- TP9: +15 V ± 0.1 V (adjustable with R6 on SWITCHING
- TP8: -15 V ± 0.1 V STABILIZER PCB 1.820.790)
- TP7: +26 V ± 1 V
- TP6: -26 V ± 1 V
- TP5: STABIN+ (unregulated voltages, variable
- TP2: STABIN- between 30 V and 63 V, depending
- TP1: CAPMOT on load and equipment of recorder)

adjusting the reference voltages:
- adjust the reference voltages on the Fuse/Supply Failure Detector PCB 1.820.737 (as a rule, only required after repairs have been made on the circuit board):
- TP4: +5.0 V ± 100 mV (adjustable with R2)
- TP12: +2.0 V ± 20 mV (adjustable with R47).

Checking the spooling motor supply voltage:
- In normal operation of the recorder, approx. + 30 V are available between the test points TP2 ("+") and TP1 ("-") on the Spooling Motor Supply PCB 1.820.777.
- The yellow LED (DL1) is dark after power on. after approx. 4 seconds it is illuminated brightly, afterwards its brightness slowly decreases to a dim glow (in normal operation).
- The red LED (DL2) is only on if the spooling motors are acting as generators and deliver energy to be dissipated by the "power Z diode" on the spooling motor control.

3.5.5 Power Supply PCM Box

* POWER ON INDICATOR
o SUPPLY VOLTAGE ADJUST

Supply voltage adjustment: measure +5 VDC voltage on the front side of the Gains Control board 1.861.853, when the board is not on an extender. Adjust this voltage with trimming potentiometer "supply voltage adjust" on the power supply to be within 4.8 .. 4.9 VDC. Check +5 VDC supply voltage on the System Controller board 1.861.763 (test point behind LED). It should be within 5.1 .. 5.3 VDC.

3.5.6 Opto Sensor 1.820.793

Checking and adjusting the switching threshold:
- Remove front half of upper tape transport cover. Then reinstall the headblock and the guide rollers.
- Connect voltmeter (range 15 VDC) to TP2 and ground (TP1).
- Switch recorder on, no tape mounted.
- If the measurement does not indicate 0 V ± 0.1 V, adjust with R27.
- Mount tape and spool forward past the leader so that magnetic tape is located in the light barrier.
- Switch recorder to STOP.
- If the measurement does not indicate 12 V at least, adjust with R26.

3.5.7 Tape Move Sensor 1.820.770

Checking and adjusting the duty cycle

- Switch recorder off.
- Remove Tape Deck Counter/Timer 1.820.761 and reinsert it via the extender board (1.820.799.00).
- Switch recorder on.
- Connect oscilloscope to terminal 7 or 8 (ground to terminal 21) of the extender board.
- Mount tape and select highest tape speed.
- Check symmetry of curve shape. The duty cycle of the two signals must be 50% ± 10%. If there are any deviations, adjust to a symmetrical square-wave signal with R3 (R3 is located next to the connector) on the Move Sensor PCB (signal on terminal 7 of the extender board) or R9 respectively (signal on terminal 8).

Phase shift of the two move signals

- The phase shift of the two square-wave signals (90° ± 10°) cannot be adjusted.

3.5.8 Mechanical Brakes

Checking the brake assembly (recorder switched off): The correct functioning of the brakes can be checked by briefly turning the spindle forward and backward. Whenever the direction changes, one of the two brake levers audibly contacts the lifting pin or the stop pin.

adjusting the brake assembly:

- Switch recorder off.
- Remove rear section of upper tape transport cover.
- The play [1] between the brake lever and its lifting pin must be 1 to 1.5 mm. adjustment procedure:
- Remove reel adapters.
- Remove spindle without brake roller, (3 screws, allen screwdriver No. 3).
- Unfasten two mounting screws [8] of the brake assembly (allen screwdriver No. 3), shift brake assembly sideways in parallel until the required play is attained. Retighten the mounting screws.
- The travel [3] of the lifting pin should be 4 to 5 mm. Check by pressing from the front against the armature of the brake solenoid. The travel can be adjusted after the two mounting screws of the brake assembly [4] (allen screwdriver No. 3) have been lightly loosened, the travel can then be adjusted by shifting the brake solenoid. Retighten the fixing screws. ■ Reinstall spindle.

adjusting the retarding torque:

- Retarding torque in take-up direction (weak braking):
- Mount empty reel with 2 to 3 m of tape in direction opposite the normal operating position.
- Hook spring dynamometer 0 - 5 N (0 to 500 p) into a loop at the start of the tape; unwind tape slowly and evenly. The retarding torque can be adjusted to the value specified in the following table by rehooking the spring [6].
- Retarding torque in supply direction (strong braking):
- Mount empty reel with 2 to 3 m of tape in normal operating position.

- Hook spring dynamometer 0 - 5 N (0 to 500 p) into a loop at the start of the tape; unwind tape slowly and evenly. The retarding torque can be adjusted by means of screw (7) to the value specified in the table below.

The retarding torque should be uniform throughout the entire length of the tape, otherwise the brake roller and the brake band need to be replaced. Before installing the brake band be sure to clean its inner surface thoroughly with spirit.

	Left-hand reel		Right-hand reel	
	Take-up direction (opposite op. pos.)	Supply direction (operating position)	Take-up direction (opposite op. pos.)	Supply direction (operating position)
1/4"	< 0.9 N (< 90 p)	2 N ± 0,15 N (200 p ±15 p)	< 0,9 N (< 90 p)	2 N ± 0,15 N (200 p ± 15 p)
1/2"	<0.9 N (< 90 p)	2 N ± 0.15 N (200 p ±15 p)	< 0.9 N (< 90 p)	2 N ± 0.15 N (200 p ± 15 p)

3.5.9 Tape Tension Sensor 1.820.772

Checking the tape tension sensor:
- Remove lower tape transport cover.
- Remove guide roller and prestabilizer roller (left) or tacho roller (right), respectively.
- Connect digital voltmeter to the two test points TP1 ("+") and TP2 (ground).
- Switch recorder on. ■ In the neutral position of the tape tension sensor (without tape) the measured voltage should be 0.000 V (+ 15 mV/- 0 mV) (Offset).
- Insert gauge for adjusting the tape tension sensors according to Fig. 3.3.9 (part No. 10.010.001.30) into the tape tension sensor; the voltage should be 2.700 V ± 10 mV (Gain).

Checking the tape tension spring: Before this check the offset and gain adjustment must be checked (see above) and adjusted, if necessary (see below).
- Install guide and prestabilizer/tacho rollers.
- Insert adjusting device (part No. 10.010.001.31) on the tape transport according to Fig. 3.3.10 (it is not necessary to remove the tape transport covers for this check).
- Connect digital voltmeter to the two test points (as above).
- Hook on small weight (20 g). The reading of the digital voltmeter should be 50 mV ±20 mV.
- Hook on the large weight (220 g). The reading of the digital voltmeter should be 3.200 V ±50 mV. If these values are not attained, the tape tension spring has to be adjusted (see below).

adjusting the tape tension sensor:

- Remove guide roller and prestabilizer roller (left) or tacho roller (right), respectively.
- Neutral position: adjust offset with R7 on TaPE TENSION SENSOR PCB (closer to the connector) to a voltage of 0.000 V (+15 mV/-0 mV).
- Insert gauge for adjusting the tape tension sensors according to Fig. 3.3.9, adjust gain with R9 to a voltage of 2.700 V ±10 mV. * Secure both potentiometer settings with locking paint.
  adjusting the tape tension spring [a]: The offset and the gain must be checked and aligned, if necessary, before this adjustment is made (see above).
- Remove front section of upper tape transport cover.
- Install guide and prestabilizer/tacho rollers.
- Install adjusting device on the tape transport (refer to Fig. 3.3.10).
- Connect digital voltmeter to the two test points (as above).
- Loosen locknut [B] of threaded pin [C].
- Hook on small weight (20 g).
- adjust the voltage to 50 mV ±20 mV by turning the threaded pin [C] (voltage increases when turning out the threaded pin).
- Tighten the locknut [B], the voltage must remain between the indicated limits.
- Hook on the large weight (220 g).
- adjust the voltage to 3.200 V ±50 mV by turning the adjusting pin [D] (voltage rises when the spring is elongated). The adjustments identified with "*" influence each other and must be repeated several times in the same sequence, if necessary.
- Secure threaded pin [C] (locknut [B]) and adjusting pin [D] with locking paint.
- Reinstall tape transport covers.

3.5.10 Pinch Unit

Checking the distance between capstan shaft and pinch roller:

- Mount tape, switch recorder on, select STOP mode.
- The distance between capstan shaft and pinch roller must measure between 0.5 and 1.0 mm. If this value is not attained, the distance is to be adjusted.

adjusting the distance between capstan shaft and pinch roller:

- Remove lower tape transport cover, tilt recorder to service position.
- Loosen locknut (opening between flats 7 mm) on the tie rod of the pinch unit and turn tie rod until the required distance between capstan shaft and pinch roller is attained.
- Retighten locknut and secure with locking paint.
- The pinch roller spring must be adjusted afterwards.

Checking the pinching force:

- Remove front section of upper tape transport cover.
- Reinstall headblock and pinch roller (without cover), unscrew fixing screw from the pinch roller cover and turn it into the tapped hole of the pinch roller shaft by 3 to 4 turns.
- Mount tape, switch recorder on, select PLay mode.
- Hook spring dynamometer 0 - 20 N to the screw, and pull in the direction of the connecting line between the centers of the capstan shaft and the pinch roller. while pulling, lightly brake the pinch roller with your finger.
- The spring dynamometer should indicate 9 N ±1 N (0.9 kp ±0.1 kp) at the point where the pinch roller just lifts off the tape (and consequently stops).

adjusting the pinching force: If this value is not attained, the pinch roller spring has to be readjusted.

- Remove lower tape transport cover, tilt recorder to service position.
- Switch recorder to PLay.
- The adjusting nut (prevailing torque type nut, opening across flats 7 mm) of the pinch unit is accessible through a hole in the cast chassis. adjust until the requested value is attained.
- Reinstall pinch roller cover after the adjustment.

3.5.11 Lifting pin

The lifting pin (between reproduce head and capstan shaft) should touch the tape only lightly in PLAY mode.

Checking and adjustment:

- Remove headblock cover (refer to 3.2.1).
- Switch recorder to PLay mode and press on the lifting pin from the front. The pin should be lifted off the tape by a few tenths of a millimeter.
- Should this not be the case, loosen the locknut (opening across flats 5.5 mm) and adjusting screw (opening across flats 5.5 mm) to such a point where the pin just touches the tape in play mode.
- Retighten locknut.
- Reinstall headblock cover.

3.5.12 Tape Tension

Check measurements: the tape tensions are measured with a Tentelometer (part No. 10.300.001.01) which is calibrated for a tape tension of 1.0 N (100 p) with 1/4" tape of the same brand used for the tape tension adjustment. The Tentelometer is to be arranged as close to the reels as possible. The tape should run perpendicularly over the center of the Tentelometer. The rear section of the upper tape transport cover may possibly have to be removed (depending on the type of Tentelometer used) in order to gain unobstructed access to the tape.

- Switch tape recorder on, select 48 kHz sampling frequency as well as a corresponding tape type (the tape tension values are also changed over when a different tape type is selected).
- Mount tape and spool forward until the tape pancakes are the same size on both reels.
- PLAY and REVERSE tape tension: the values specified in the table below must be attained. when the pinch roller is manually lifted slightly off the tape, the reels should stand still after one full revolution at the most. The service display should indicate the following message:

```
ERR: PINCH ROLLER
     SLIPPING
```

(after having released the pinch roller, this message disappears)

- Spooling tension:
  to check the tape tension in spooling mode, the winding speed is to be set to 0.5 m/s:
- Open the programming lock (allen screwdriver No. 2.5, approx. one turn in the counterclockwise direction).
- Starting with the display status "L RaNGE ./. dBm", press ↓/NEXT twice, →/CURSOR once, and ↓/NExT four times in order to page forward to the block "SET Max wIND SPEED".

- Set the parameter to 0.5 m/s with the SET/CUE wheel.
- Press STORE.
- Press ↑/LaST six times.
- Measure on the left-hand reel, function ►. The values specified in the following table should be attained.
- Restore the original winding speed (same procedure as above).
- Close programming lock (turn to the clockwise stop).
- STOP and EDIT tape tension:
- Switch tape recorder to STOP.
- Measure on left-hand reel. During the measurement, manually turn the right-hand reel counterclockwise slowly and evenly.

	1/4"	
	Left	Right
PLay	1,0 N ±0,1 N 100 p ± 10 p	1,3 N ±0,1 N 130 p ± 10 p
<>	1,0 N ±0,1 N 100 p ± 10 p	---- ----
STOP EDIT	1,0 N ±0,1 N 100 p ± 10 p	---- ----

Tape tension adjustments: These values must be corrected if they are not attained.

- Open the programming lock (allen screwdriver No. 2.5, approx. one turn in the counterclockwise direction).
- Starting with the display status "L RANGE ./. dBm", press ↓/NEXT twice, →/CURSOR once, and ↓/NEXT several times for the PLay tape tension, the spooling tape tensions, and the STOP/EDIT tape tension, in order to page to the desired programming blocks. Changeover right/left with →/CURSOR or ←/CURSOR (indication in the LC display). The selected tape type is also displayed (upper right section of the LC display), the changeover is performed by pressing STOP and TAPE A/TAPE B at the same time.
- Set the parameter to the desired value with the aid of the SET/CUE wheel. The values displayed in the LCD display of the D820X correspond to decimal numbers without unit, compared to the A820 where hex numbers are displayed. The numbers have no direct relationship with the actual tension value.
- Press STORE.
- Press ↑/LAST as often as required so that the service display indicates "L RANGE ./. dBm".
- Close programming lock (turn to the clockwise stop).

3.5.13 Exchanging the Headblock Assembly

Important: To prevent unwanted magnetization of the heads, the recorder must be switched off before the headblock is removed or reinstalled.

Remove the pressure roller and unfasten three screws (allen No. 3 for all of them) holding the headblock assy. The three screws are located in front of the left tape guidance, to the right of the pressure roller and one behind the headblock cover. all are accessible from top.

Then remove the cover over the cage electronics behind the headblock (2 allen No. 2.5 screws) and disconnect the flexi PCB from the write head to the write amplifier. This is a 26 way flatcable connector. The header type on the write amplifier contains latching levers which are to be pressed outside.

Hold the headblock assembly at its cover and pull carefully. Make sure that the flexi PCB at the rear side is not damaged during transportation.

Scrape flutter roller The scrape flutter roller can be removed after the screw [M] accessible from the bottom (allen screwdriver No. 2.5) has been unfastened. The height adjustment of the scrape flutter roller does not need to be checked after removal of the roller because the height has been aligned exactly by the factory. adjusting the tape guidance elements Check the left-hand ceramic tape guide (between the erase and the record head) with the aid of the tape guidance alignment gauge (part No. 10.xxx.xxx.xx).

3.5.14 Capstan Motor

The capstan motor 1.021.601.00 operates under the control of the Capstan Control Unit 1.820.764 . The assembly 1.820.764 is used in conjunction with motor 1.021.601.81.
Capstan motor tacho.
The capacitive scanners as well as the three Hall effect sensors can only be adjusted in the factory.

Tacho Sensor Electronics PCB 1.021.695.81

- Remove capstan motor (refer to 3.2.13), but leave it connected. Remove the TaCHO SENSOR ELECTRONICS PCB 1.021.695.81 from the capstan motor (2 screws, allen screwdriver No. 2.5)
- Switch recorder on, without tape. Tape speed 15 ips.
- Start capstan motor by pressing PLay.
- Connect frequency counter to TP2 (ground lead to TP1).
- Set oscillator frequency with L1 to 5.5 MHz ±500 kHz.
- Connect oscilloscope (possbily aF voltmeter) to TP4 (ground lead to TP1).
- adjust for maximum amplitude with L3.
- Connect oscilloscope (possibly aF voltmeter) to TP3 (ground lead to TP1).
- adjust for maximum amplitude with L2.
- Connect oscilloscope to signal TD-TCM2 (IC1/pin 2) and adjust with R41 to duty cycle of 50%. The following adjustments can or have to be executed with the capstan motor installed (trimmer potentiometer R41 is accessible from below if the bottom cover is removed):
- If a wow-and-flutter meter is available, reinstall the capstan motor.
  Minimize the linear wow and flutter with R41.

- By way of expedient this adjustment can also be made in one of the two following ways:
- with oscilloscope (with removed capstan motor only):
  Connect oscilloscope to TP3 (ground lead to TP1).
  adjust signal with R41 to minimum jitter.
- By ear (also possible with reinserted capstan motor): Press blade of a large screwdriver (approx. No. 6) against the capstan motor housing. with one ear listen to the motor noise on the screwdriver handle and minimize loudness with R41.

Caution: tape speed may slightly differ due to variations of capstan shaft diameter after exchange. The speed variation will be inaudible, the head distance, however, may not be correct anymore, impairing sync recording mode. Check head distance after replacement of capstan motor!

3.5.15 Spooling Motor Tacho 1.820.771 GRP36 (left), GRP37 (right)

Checking and adjusting the duty cycle

- Plug in Tape Deck Counter/Timer PCB 1.820.761 via the extender board (Part No. 1.820.799.00).
- Connect oscilloscope to terminal 1 or 2 (left-hand motor), terminal 3 or 4 (right-hand motor), and ground lead to terminal 21 of the extender board.
- Mount tape, switch recorder to spooling mode.
- Check symmetry of wave form. The duty cycle of the signals (two for each motor) should be 50% ± 10%. Corrections to a symmetric square-wave signal can be made with the trimmer potentiometers on the corresponding Spooling Motor Tacho PCB (see table).

	Left-hand motor tacho		Right-hand motor tacho	
Trimmer potentiometer	R11	R12	R11	R12
Pin on extender board	1	2	3	4

Phase shift of the two signals The phase shift (90°) of the two square-wave signals is factory aligned and cannot be adjusted.

3.5.16 Cue Sensor (Edit Assembly) 1.820.765

SET/CUE wheel, check and adjustment of the duty cycle

- Remove lower tape transport cover.
- Connect oscilloscope to TP1 or TP2 respectively, ground lead to TP3 of the Cue Sensor PCB.
- Switch recorder on.
- Turn SET/CUE wheel as steadily as possible.
- Check the symmetry of the wave form. The duty cycle of the two signals should be 50% ± 10%. Corrections to a symmetric square-wave signal can be made with R1 on the Cue Sensor PCB (signal on TP1 of the Cue Sensor PCB) or R12 (signal on TP2).

SHUTTLE wheel, check of center position
Prerequisite: the SHUTTLE wheel returns easily to its center position from both directions.

- Remove lower tape transport cover.
- Mount tape, switch recorder on.
- Check that the "dead" range of the SHUTTLE wheel is symmetrical to the neutral position.
- For this behalf, connect digital multimeter (range 10 V DC, display capacity at least two digits on the right of the decimal point) to the SHUTTLE potentiometer (+ ≙ red wire; ground ≙ brn wire).
- Turn SHUTTLE wheel to the right until the tape starts moving, note the multimeter reading.
- Turn SHUTTLE wheel to the left until the tape starts moving, note the multimeter reading.
- Compute the mean value of the two readings.
- Measure the voltage in the center position of the SHUTTLE wheel. The reading must correspond to the computed value. Should this not be the case, the assembly must be removed, but reconnected for adjustment.

SHUTTLE wheel, adjustment of the center position

- Lightly loosen the headless screw on the small toothed wheel (on the potentiometer shaft).
- Hold the SHUTTLE wheel in the center position and turn the potentiometer shaft with the aid of a screwdriver until the correct value is attained.
- Recheck after the headless screw has been tightened.
- Reinstall the assembly.

3.5.17 LC Display Unit 1.861.233

The contrast of the LC display can be optimized for different viewing angles.

- Remove front half of top cover (see 3.2.2).
- Optimize the contrast for the preferred viewing angle with the trimmer potentiometer R1 on the connector PCB 1.820.797 (if the front half of the top cover is removed, R1 is accessible from above or, for preceding assemblies, respectively, from the tape tension sensor).

3.5.18 Adjustments and Test Points on the PCBs Tape Transport Control

Reference voltages for D/A converters: as a rule, these adjustments are only necessary after the corresponding PCBs have been repaired. Component arrangement drawings can be found in the diagram Section.

- Tape Deck Serial Interface PCB 1.820.763:
  with R36, adjust TP2 to +5.0 V ± 10 mV (relative to TP1).
- Spooling Motor Controller 1.820.760:
  with R34, adjust TP2 to -5.0 V ± 10 mV (relative to TP1).
- Capstan Interface PCB 1.820.727:
  with R12 adjust TP1 to +10.0 V ± 10 mV (relative to TP2).

Test points:

- Tape Deck Periphery Controller 1.820.762:
  The two test points TP1 and TP2 are only used during production for checking the assembly.

- Spooling Motor Drive Amplifier 1.820.775
  - TP1: Ground.
  - TP2: Voltage proportional to the motor current (16 a ≙ 5 V or 1 a ≙ 312.5 mV).
  - TP3: Ground.
  - TP4: Pulse-width-modulated control signal for motor power stage.
- Capstan Motor Drive Amplifier 1.820.774:
  - TP1: Ground.
  - TP2: Dirac pulse, TTL level, 76 kHz.
  - TP3: Pulse-width-modulated signal, amplitude 0 to 50 V (relative to ground), voltage depends on capstan motor speed, 76 kHz.
  - TP4: DC voltage, mean value of the voltage on TP 3, 0 - 50 V.
  - TP5, TP6, TP7: 120° phase-shifted aC voltages. waveform: sinusoidal, approximated by means of trapezoides.
  - TP8: Square-wave signal, TTL level, combination of the output signals of the three Hall effect sensors (triple frequency).

3.5.19 Calibration of Analog In- & Output

1.861.571.20:

R 57/157: level correction DAC
R 95/ 96: level adjust

1.861.752/3.20:

R 113/213: CMRR (input w/o transformer)
R 108/208: level adjust
R 131/231: gain 2nd conversion
R 132/232: gain 1st conversion
R 140/240: offset
R 145/245: level correction DAC

3.6
Removing Assemblies

3.6.1
Power Supply, Tape Transport Control

3.6.1.1

Access to Transport Assemblies

- Open the flap on the amplifier bay: unfasten the stop screw (allen screwdriver No. 3). Open flap with a sharp pull.
- Folding down the amplifier bay: unfasten two stop screws (allen screwdriver No. 3). Lightly lift the amplifier bay and press the button in the middle of the bay to release the catch. We recommend to manually cushion the amplifier bay as it swings out. when closing the bay it is necessary to lightly lift the latter and to push the stop lever back so that the bay can be engaged with some momentum.

For measuring the weighted and linear signal-to-noise ratio and the RF ratios, the amplifier bay must be closed and the three stop screws tightened.

Warning Disconnect power plug before removing any housing panels.

3.6.2
Headblock Assembly

Head cover

- Unfasten two screws [a] (allen screwdriver No. 3).

Headblock (with headblock cover)

Important! To prevent unwanted magnetization of the soundheads, the recorder must be switched off when the headblock is being removed.

It is not necessary to remove the head cover for removing the headblock.

- Remove pinch roller (allen screwdriver No. 3).
- Unfasten three screws (accessible through holes [B] in the soundhead or headblock cover) with the aid of the allen screwdriver No. 3.
- Carefully lift off the headblock so that the capstan shaft will not become damaged.

Caution: **head distance must be checked after exchange of capstan motor!**

3.6.3 Covers

Upper tape transport cover, rear section
- Unfasten seven screws (allen screwdriver No. 2.5).
- Lift off cover.

Upper tape transport cover, front section
- Remove pinch roller, prestabilizer roller (left), and guide roller (on the right of the headblock) by unfastening one screw each (allen screwdriver No. 3). IMPORTaNT: The height of the rollers might be adjusted with shims - neither confuse or lose the shims, if any.
- Remove headblock (refer to 3.2.1).
- Unfasten seven screws (allen screwdriver No. 2.5).
- Lift off cover.

Please note during reinstallation procedure:
- Install prestabilizer roller (heavy) on the left-hand side, guide roller (light) on the right-hand side of the headblock.
- The covers of the prestabilizer roller and the guide roller must be mounted correctly: protected against orientation confusion.

Tape transport cover, bottom
- Unfasten eleven screws (one below the release lever for console swiveling mechanism; allen screwdriver No. 2.5).

Rear panel
- Unfasten five screws (allen screwdriver No. 2.5).

Power supply cover
- Unfasten ten screws (allen screwdriver No. 2.5).

wooden side panels
- Unfasten four screws each (allen screwdriver No. 4).

3.6.4 Push Button Rail

- Unscrew front section of upper tape transport cover as well as the lower tape transport cover (refer to 3.2.2).
- Disconnect 40-pin flat-cable connector on Tape Deck Display Driver PCB.
- Unfasten two screws (allen screwdriver No. 2.5).
- Carefully lift off push button rail.

3.6.5 Tape Transport Push Button Assembly

- Remove push button rail (3.2.3).
- Disconnect flat-cable connector on the left-hand edge of the Tape Deck Display Driver PCB. Open cable clamp in which the flat cables are secured.
- Unfasten two screws [C] (allen screwdriver No. 3).

3.6.6 Service Display

- Remove push button rail (3.2.3).
- Detach flat-cable connector on the top edge of the Tape Deck Display Driver PCB.
- Unfasten two screws [D] (allen screwdriver No. 2.5).

3.6.7 Tape Guide Assembly

- Remove front section of upper tape transport cover (3.2.2).
- Slide two slot covers [E] over the shaft stubs of the prestabilizer roller and guide roller and slide them as far as possible in the direction of the brake solenoids.
- Unfasten three screws [F] (allen screwdriver No. 3).
- Remove assembly. Do not turn upside down, otherwise the three screws will drop out.

Please note during reinstallation procedure:

- Manually turn the two cam discs (on the shafts of the synchronous motors) to their clockwise limit positions.
- Lightly twist clockwise the swivel arm of the prestabilizer roller and the one of the ceramic tape guide as well as counterclockwise the swivel arm of the guide roller, and carefully insert the tape guide assembly.
- Lift the two slot covers over the shaft stubs and ensure that the shaft end [G] of each swivel arm fits into the small hole [H] of the shields.

3.6.8 Tape Tension Sensors

- Remove headblock (3.2.1), front section of upper tape transport cover, and lower tape transport cover (3.2.3).
- Detach flat-cable connector on the underside of the tape tension sensor.
- Unfasten three special screws for each tape tension sensor (ball head allen screwdriver No. 3), accessible through the cutout at the sleeve edge of the guide roller.

3.6.9 Tape End Sensor (Light Barrier) with Guide Roller

- Remove headblock (3.2.1) and front section of upper tape transport cover (3.2.3).
- Detach flat-cable connector on the sensor PCB.
- Unfasten three special screws (allen screwdriver No. 3).

3.6.10 Tape Move Sensor

- Remove headblock (3.2.1) and front section of upper tape transport cover as well as lower tape transport cover (3.2.2).
- Detach flat cable connector on the underside.
- Unfasten three special screws (allen screwdriver No. 3).

3.6.11 Spindle (incl. Brake Roller)

- Remove rear section of upper tape transport cover.
- Disengage adapter by pressing down the ring at the edge of the spindle and remove it.
- Unfasten screw in the center of the spindle (allen screwdriver No. 4).
- By pressing against the armature of the brake solenoid (see arrow), release the brake band from the brake lining to such an extent that the spindle can be lifted off without twisting the brake band.

Important! The height of the brake drum has been adjusted with shims. Do not lose or confuse the shims. Neither the inside of the brake band nor the brake lining (reddish fabric) should be touched with your fingers.

- when reinstalling the spindle, also ensure that the brake band does not become twisted: release the band by pressing against the armature of the brake solenoid.

3.6.12 Tape Brakes

- Remove spindle (3.2.10).
- Detach the supply cable to the brake solenoid.
- Unfasten two screws (allen screwdriver No. 3).
- During removal, guide the supply cable of the brake solenoid through the tape transport chassis.

Please note during reinstallation procedure:
- Insert supply cable of the brake solenoid.
- adjust brake chassis (refer to 3.3.4).

3.6.13 Spooling Motors

- Remove spindle (3.2.10).
- Remove stop plate for brake band (2 screws [J], (allen screwdriver No. 3).
- Remove lower tape transport cover (3.2.2).
- Detach motor supply cables on Spooling Motor Drive Amplifier PCB and flat cable on Motor Tacho PCB (behind motor).
- Unfasten three screws [K] (allen screwdriver No. 4). To prevent the motor from falling out, it must be supported from the bottom while the screws are being unfastened.
- Ensure that the polarity is correct when you reinstall the motor. Red ≙ "+" (or "B" on the left-hand spoolingmotor, "a" on the right-hand spooling motor).

3.6.14 Capstan Motor

The capstan motor 1.021.601.00 operates under the control of the Capstan Control Unit 1.820.764.00/.20. The assembly 1.820.764.21/.22 is used in conjunction with the motor 1.021.601.81.

- Remove front section of upper tape transport cover and lower tape transport cover (3.2.2).
- Detach multipin connector (Molex) on Capstan Motor Drive Amplifier.
- Unfasten three special screws (allen screwdriver No. 3). To prevent the motor from dropping out, it must be supported from the bottom while the screws are being unfastened.

Caution: **tape speed nay slightly differ due to variations of capstan shaft diameter after exchange. The speed variation will be inaudible, the head distance, however, may not be correct anymore, i,pairing sync recording mode. Check head distance after replacement of capstan motor!**

3.6.15 Power Supply

- Remove power supply cover, rear section of opper tape transport cover, and lower tape transport cover (3.2.2).
- Unscrew power switch (allen screwdriver No. 3).
- Detach one cable harness each (in a gray plastic tube) from the Stabilizer/Limiter PCB, from the Spooling Motor Supply PCB and from the power switch. Unfasten cable clamp of the cable harness to the power switch (allen screwdriver No. 3).
- Open and empty cable duct.
- Detach connectors of the two stranded ground wires (blk).
- Unfasten eleven screws (allen screwdriver No. 2.5) at the lower edge of the connector panels. Remove remote-control connector panel by unfastening three additional screws.
- Unplug stranded ground wire blk (connector on Parallel Remote Interface PCB).
- Detach flat-cable connection on Parallel Remote Interface, pull circuit board out of the guide rails, detach second flat-cable connection.
- Unfasten three screws each on the left-hand and right-hand side panel of the amplifier bay. Hold the power supply unit while you unfasten the screws.
- Carefully lift out the power supply unit.

Reinstallation procedure

- all still existing connector panels and filler panels are to be removed completely before commencing with the reinstallation (6 additional screws, allen screwdriver No. 2.5).
- The reinstallation procedure can subsequently be started by performing the foregoing steps in the reverse order.
- Reconnecting the power switch: 2 x blu in the middle, 2 x brn on the narrow side of the power switch.

3.6.16
Spooling Motor Drive Amplifier, Spooling Motor Supply

- Remove rear cover (3.2.2), swing down amplifier bay, and set recorder into service position.
- Connections:
  - Spooling Motor Drive Amplifier: Two motor supply conductors (AMP terminals; red ≙ "+", blk ≙ "-"), one flat-cable connector and one Molex connector.
  - Spooling Motor Supply: Detach one flat-cable connector and three Molex connectors.
  - Stabilizer/Limiter: Detach two Molex connectors.
- Each of the four assemblies is secured on the back of the recorder by means of a screw (allen screwdriver No. 3). The assembly can be removed toward the rear after this screw has been unfastened.
- Upon reinstallation, the two pins (on each assembly) must fit into the corresponding holes of the recorder chassis.