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TI 76/89
Time code reader chip STUDER TCIA

10.85.1300 (Ed.1189)

Technical Information

APPLICATION NOTES

1. General

The TCIA accepts SMPTE/EBU longitudinal Time Code as input and produces both 8-bit parallel and serial data as output.

The TCIA will accept SMPTE/ EBU LTC at speed from 1/100 to 100 times play speed. It can be directly connected either to the Motorola 6800/6803 or the Intel 8080/8088 MPU Bus with no additional circuitry.

In the stand alone mode (without MPU) the TCIA can be used in conjunction with the Motorola MC14449 7-Segment LED Display Driver to display the Time Code or User Bits Data.

I/O signals:

- SMPTE/EBU LTC input,
- 8 bit data output
- serial data and 8-bit parallel data outputs
- the following status information of the incoming time code data are available to the MPU by reading the TCIA Status Register:
  - TC - Overflow
  - TC - Underflow
  - TC - Clock validity
  - TC - Direction

- parallel data outputs are asynchronous with the input TC allowing data to be output at any rate
- user selectable output of either TC Data or User Bit Data by the external adress inputs
- tape speed can be determined by reading the TCIA 16-bit Time Code Period Register (Motorola MPU mode only)
- perfect error recognition and supression of invalid frames.

2. TCIA operation

Receive Shift Register

The Receive Shift Register is a 64-bit bidirectional serial input/parallel output shift register. The content of the Receive Shift Register is a complete time code word (Time code and user bits)

TC - data buffer, UB - data buffer

The TC - Data Buffer consists of 4 read-only 8-bit registers (Frames, Seconds, Minutes, Hours).

These registers are selected when RS, R/W and A2 are "high". The 4 registers of the UB - Data Buffer are selected when RS and R/W are "high" and A2 is "low".

Data Buffer Register select truth table

CONTROL INPUTS:	RS	A2	A1	A0	REGISTERS
TC - Data Buffer	1	1	1	1	Frames
	1	1	1	0	Seconds
	1	1	0	1	Minutes
	1	1	0	0	Hours
UB - Data Buffer	1	0	1	1	UB - Groups 1,2
	1	0	1	0	" 3,4
	1	0	0	1	" 5,6
	1	0	0	0	" 7,8

Upon receiving a complete time code word, data are automatically transferred from the Receive Shift Register to the TC and UB - Data Buffers. This event causes the Receive Data Buffer Full Bit of the Status Register to be set to "1" (full). A read cycle of the Frame Register causes the Receive Data Buffer Full Bit to be cleared.

Note that the random access to the TC or UB - Data Buffer Registers is possible but the Frames Register must be accessed at the end of a read sequence to guarantee that the Receive Data Register Full Bit will be cleared.

The data transfer from the Receive Shift Register to the TC and UB - Data Buffers will be inhibited as long as the Receive Data Full Bit is set to "1".

Control register

The TCIA Control Register consists of 5 bits of write-only buffer that are selected when RS and R/W are "low".

Bit 0: **Reset.**
This bit is used to provide a MASTER RESET for the TCIA which clears the Status Register and the Receive Data Register. Bit 0 must be set to "1" to reset the TCIA.

The TCIA releases the Master Reset automatically after a time of max 50 us.

Bit 4: **Mode.**
This bit is used to provide the Operating Mode Select for the TCIA. If this bit is set "0", the TCIA will be programmed to operate in the STAND ALONE MODE. In this mode the TCIA will be used in conjuction with the Motorola MC14449 7-Segment LED Driver to display the Time Code or User Bits Data. The applications example is shown in Fig.1.

The outputs TC-CLK, TC-DATA, /EN1, /EN2 are used to control the MC14449 Display Driver. In addition, the /IRQ output indicates in the Stand Alone Mode the Drop Frame Format of the Time Code and the input A0 indicates whether the Time Code Data or the User Bits Data is to be transferred to the Display Driver. After Power On or Software Reset, bit 4 will be set and enables the TCIA to operate in the STAND ALONE MODE.

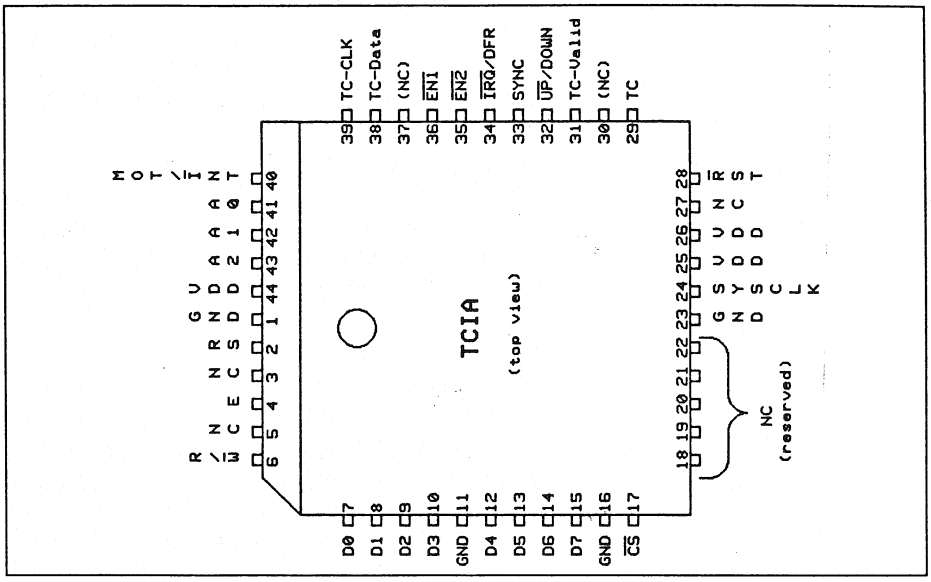


Fig. 1

Bit 5: **TC-Underflow Interrupt Enable**
If this bit is set, the TC-Underflow Interrupt will be enabled.

Bit 6: **TC-Overflow Interrupt Enable**
To enable the TC-Overflow Interrupt, this bit must be set.

Bit 7: **Receive Interrupt Enable**
The following interrupts will be enabled by a "1" in bit position 7 of the Control Register: Receive Data Buffer Full and Receive Data Buffer Overrun.

Status register

Information on the status of the TCIA is available to the MPU by reading the TCIA Status Register. This read - only register is selected when RS, A0 and A1 are "low" and R/W is "high".

Bit 0: **Receive Data Buffer Full, bit 0**
Bit 0 being set "1" indicates that the complete received data (TC-Data and User Bits Groups) has been transfered to the TC-Data Buffer and UB-Data Buffer. Bit 0 is cleared after an MPU read of Data Buffer(s) has been completed by reading the Frames Register or by a Master Reset.

Bit 1: **Receive Buffer Overrun, bit 1**
Overrun is an error flag that indicates that one or more TC-Frames in the data stream were lost. That means a TC-Frame or a number of frames were received but not read from the Receive Data Buffer(s) prior to subsequent frames being received. The transfer of the overruning frame into the Receive Data Buffers will be inhibited. This error causes the bit 1 of the Status Register to be set to "1". The overrun status flag is reset after the reading of the data from the Receive Data Buffers or by a Master Reset.

Bit 2: **TC - Period Bit 16, bit 2**
The bit 2 position of the Status Register contains the most significant bit (bit 16) of the TC - Period Data (see TC - Period Register, page 4)

Bit 3: **Time Code Direction**
The forward direction of the Time Code is indicated by a "0" in the bit position 3 of the Status Register, a "1" indicates the reverse direction. The Master Reset causes the Time Code Direction Bit to be cleared (forward).

Bit 4: **Time Code Clock Valid**
The Time Code Clock Valid Bit of the Status Register will be "1" when a valid Time Code Clock is present at the TC-CLK output of the TCIA. This bit will be cleared in the case of improper TC-CLK recovering (TC-Overflow,TC-Underflow,dropouts in the Time Code signal) or by a Master Reset.

Bit 5: **TC - Underflow**
TC-Underflow is an error flag which indicates that the rate of the incoming serial Time Code Data is to low. In addition, the underflow flag is used to indicate that one or more data bits of the Time Code signal were lost (dropouts). The underflow condition will be indicated by a "1" in bit position 5 of the Status Register. The TC-Underflow bit remains set until the next valid TC-Frame synch-word is decoded. Master Reset causes the TC-Underflow bit also to be cleared.

Bit 6: **TC - Overflow**
The TC-Overflow bit being set "1" indicates that the rate of the incoming serial Time Code Data is to high for the proper TC-CLK recovering and the Time Code Data decoding. This bit remains set until the next valid TC-Frame synch-word is decoded. It will be cleared also by the Master Reset.

Bit 7: **Interrupt Request**
The IRQ bit indicates the state of the /IRQ output of the TCIA. Any interrupt condition with its applicable enable will be indicated in this status bit. Anytime the IRQ output is "low" the IRQ bit will be "1" to indicate the interrupt or service request status. The IRQ bit is cleared by a read operation to the Status Register or by the Master Reset.

TC - Period Register

The TC-PERIOD REGISTER is a 16-bit read only register. This register contains the number of the SYSCLK pulses per one Time Code Bit Period divided by 2. This data can be used for the instantaneous tape speed calculation. The LSB and MSB of the TC-Period Register will be selected by the address input lines A0 and A1 if RS is "low" and R/W is "high":

A1	A0	
0	1	LSB
1	0	MSB

During the MPU read operation of the TC-Period Register the MSB must be read first. After the MSB read cycle, the update of the TC-Period Register will be inhibited until the read operation has been completed by reading the LSB.

Note: The TC-Period is a 17-bit binary number. The most significant bit (bit 16) is transfered to the Status Register (see Status Register, bit 2).

The TC - PERIOD REGISTER is only readable in Motorola Timing Mode!

3. Interface signals for the MPU

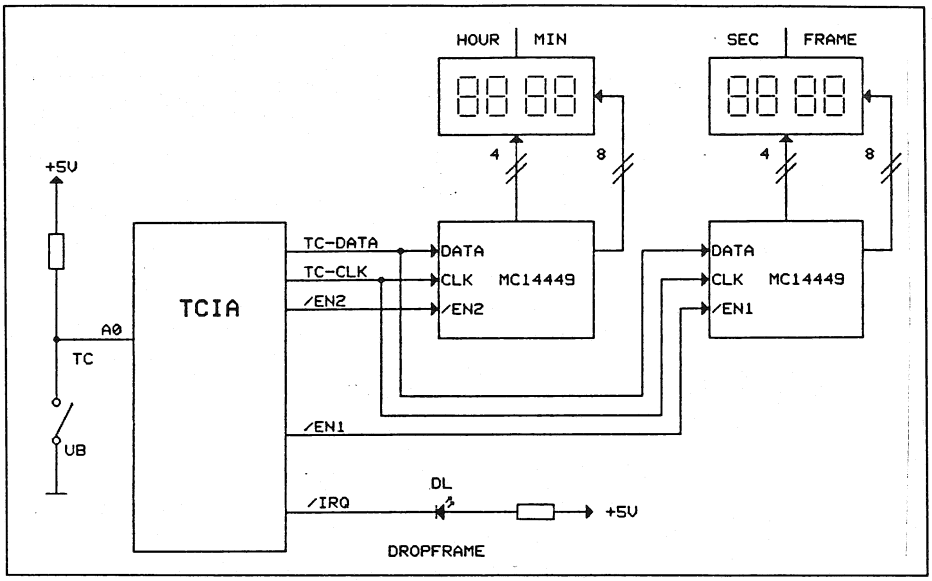


Fig. 2

Bi-Directional Data Bus (D0 - D7)

The bi-directional data bus (D0 - D7) allow for data transfer between the TCIA and the MPU. The data bus output drivers are three-state devices that remain in the high impendance (off) state except when the MPU performs a TCIA read operation.

Enable (E)

This high impedance TTL compatible input depends on the selected MPU timing mode (see Fig. 3 / Fig. 4):

Intel: This signal indicates a read operation. When the TCIA is selected via /CS the E signal enables the bus drivers to send data from an internal register on the Data Bus.

Motorola: The E signal enables the bus input/output data buffers and clocks data to and from the TCIA. This signal will normally be a derivative of the 6800/6803 MPU Clock.

Read/Write (R/W)

This high impedance TTL compatible input depends on the selected MPU timing mode (see Fig. 3/4).

Intel: This signal indicates a write operation. When /CS is active the TCIA loads an internal register with data provided via the Data Bus.

Motorola: This signal is used to control the direction of data flow through the TCIA's input/output data bus interface. When R/W is "high" (MPU Read cycle), TCIA output drivers are turned on and a selected register is read. When it is "low", the TCIA output drivers are turned off and the MPU writes into a selected register.

Therefore,the R/W signal is used to select read-only or write-only registers within the TCIA.

Chip Select(/CS)

This high impedance TTL compatible input line is used to enable the TCIA. If /CS is "low", data transfer will be performed under the control of E, R/W, RS, and the address lines A0, A1, and A2.

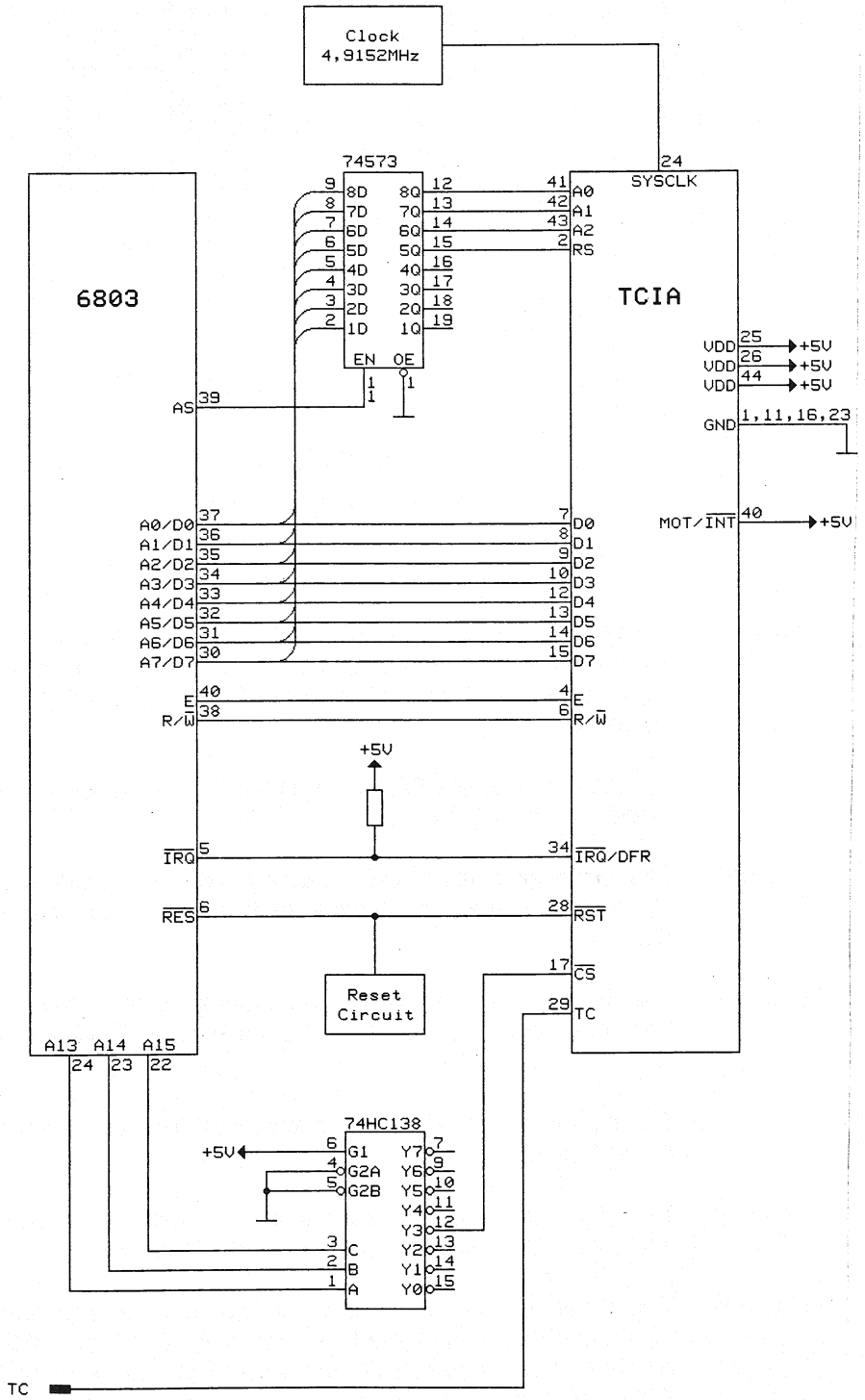

Clock
4,9152MHz
74573
6803
TCIA
SYSCLK
AS
A0/D0
A1/D1
A2/D2
A3/D3
A4/D4
A5/D5
A6/D6
A7/D7
E
R/W
IRQ
RES
MOT/INT
+5V
GND
Reset
Circuit
A13 A14 A15
74HC138
TC

Fig. 3

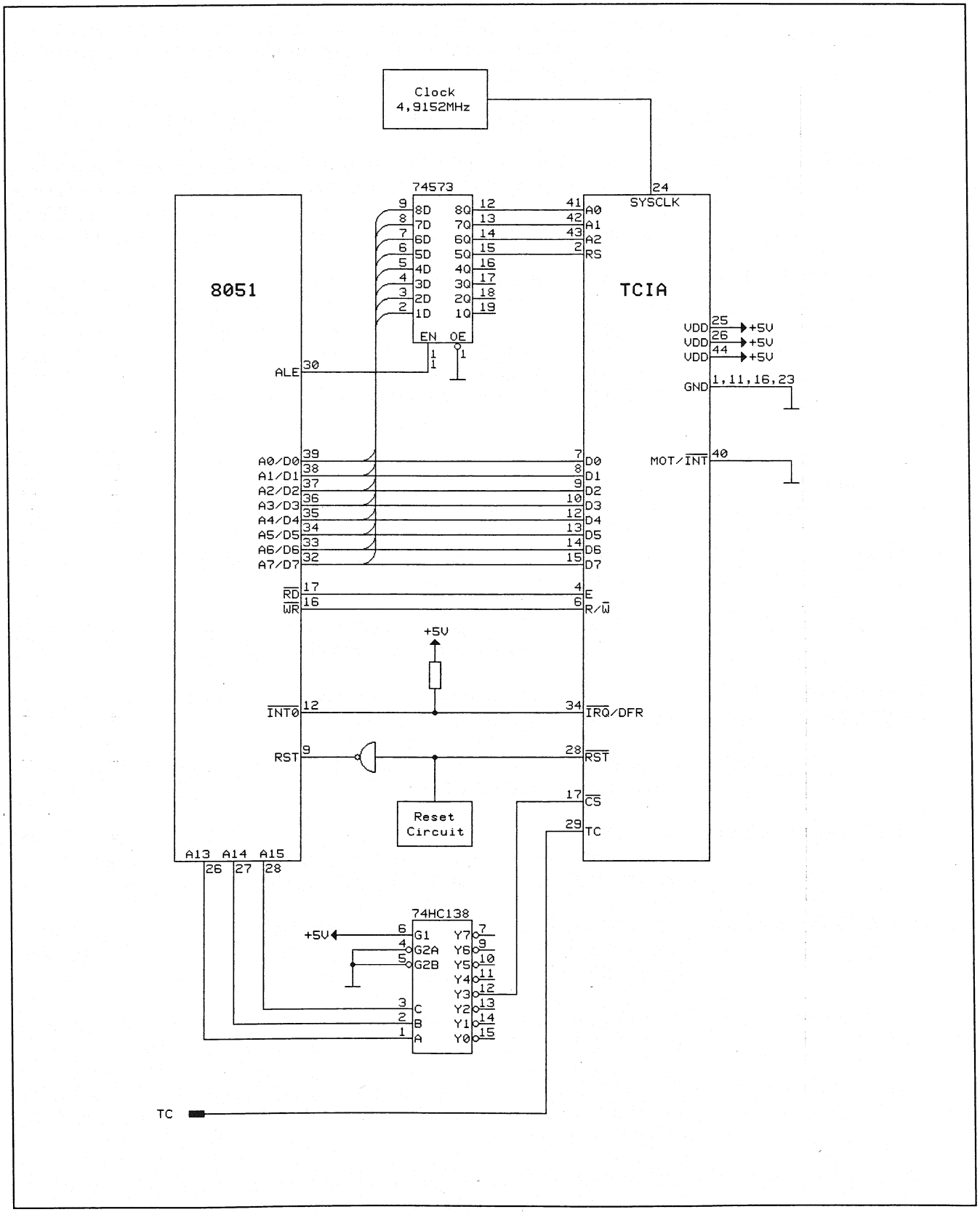

Clock
4,9152MHz
74573
8D 8Q
7D 7Q
6D 6Q
5D 5Q
4D 4Q
3D 3Q
2D 2Q
1D 1Q
EN OE
8051
TCIA
SYSCLK
A0
A1
A2
RS
VDD +5V
VDD +5V
VDD +5V
GND 1,11,16,23
MOT/INT
ALE
A0/D0
A1/D1
A2/D2
A3/D3
A4/D4
A5/D5
A6/D6
A7/D7
D0
D1
D2
D3
D4
D5
D6
D7
RD
WR
E
R/W
+5V
INT0
IRQ/DFR
RST
Reset
Circuit
CS
TC
A13 A14 A15
74HC138
G1
G2A
G2B
C
B
A
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
TC

Fig. 4

Register Select(RS)

The RS line is a high impedance TTL compatible input. A "high" level is used to select the Receive Data Registers and a "low" level the Control/Status Registers. The R/W signal line is used in conjunction with Register Select to select the read-only or write-only registers in each register pair.

Note: The TC-PERIOD REGISTER will be addressed, if RS is "low" !

Data Register Select (A0, A1, A2)

The A0, A1, A2 are TTL compatible input lines used to select which data is present at the data outputs D0 - D7. In the stand alone mode a "low" level at the input A0 causes the User Bits Data to be transferred to the MC14449 Display Drivers. A "high" level at the input A0 enables the display of the Time Code Data (see Fig. 2):

Interrupt Request(/IRQ)

/IRQ is a TTL compatible, open drain (no internal pull-up), active "low" output that is used to interrupt the MPU. The /IRQ output remains "low" as long as the cause of the interrupt is present and the appropriate interrupt enable bit within the TCIA is set. In the stand alone mode, the /IRQ output is used to indicate the dropframe format of the Time Code. The /IRQ output remains "low" as long as the dropframe bit of the incoming Time Code Data is set "1".(see Fig. 2).

4. TCIA inputs and outputs (except MPU interface signals)

/RST Reset

In the "low" state, the TTL compatible input /RST causes a Master reset for the TCIA (see Fig. 5).

SYSCLK System Clock

SYSCLK is the TTL compatible input used for the Time Code Clock recovering and the Time Code Data decoding (normally 4,9152 MHz).

MOT/INT Motorola/Intel Timing Switch

A "high" at this TTL compatible input means, that the Motorola Timing Mode is desired. A "low" selects the Intel Timing Mode.

Note: If this input is not connected to a logical state it will be driven automatically to "high" (internal pull up, see table 1).

TC - CLK Time Code Clock

TC - CLK is a TTL compatible output for the Time Code Clock which is derived from the incoming Time Code. In the stand alone mode the output TC - CLK is used to clock the data in the MC14449 Display Drivers (see Fig. 2).

TC - DATA Time Code Data

TC - DATA is a TTL compatible output which transfers the decoded Time Code Data in the serial NRZI format. Additionally, in the stand alone mode this output is used to drive the MC14449 data inputs (see Fig. 2).

/EN1,/EN2 Enable 1, Enable 2

These two TTL compatible outputs are used in the stand alone mode only. They control the data transfer from the TCIA to the MC14449 (see Fig. 2).

TC - SYNC Time Code Sync

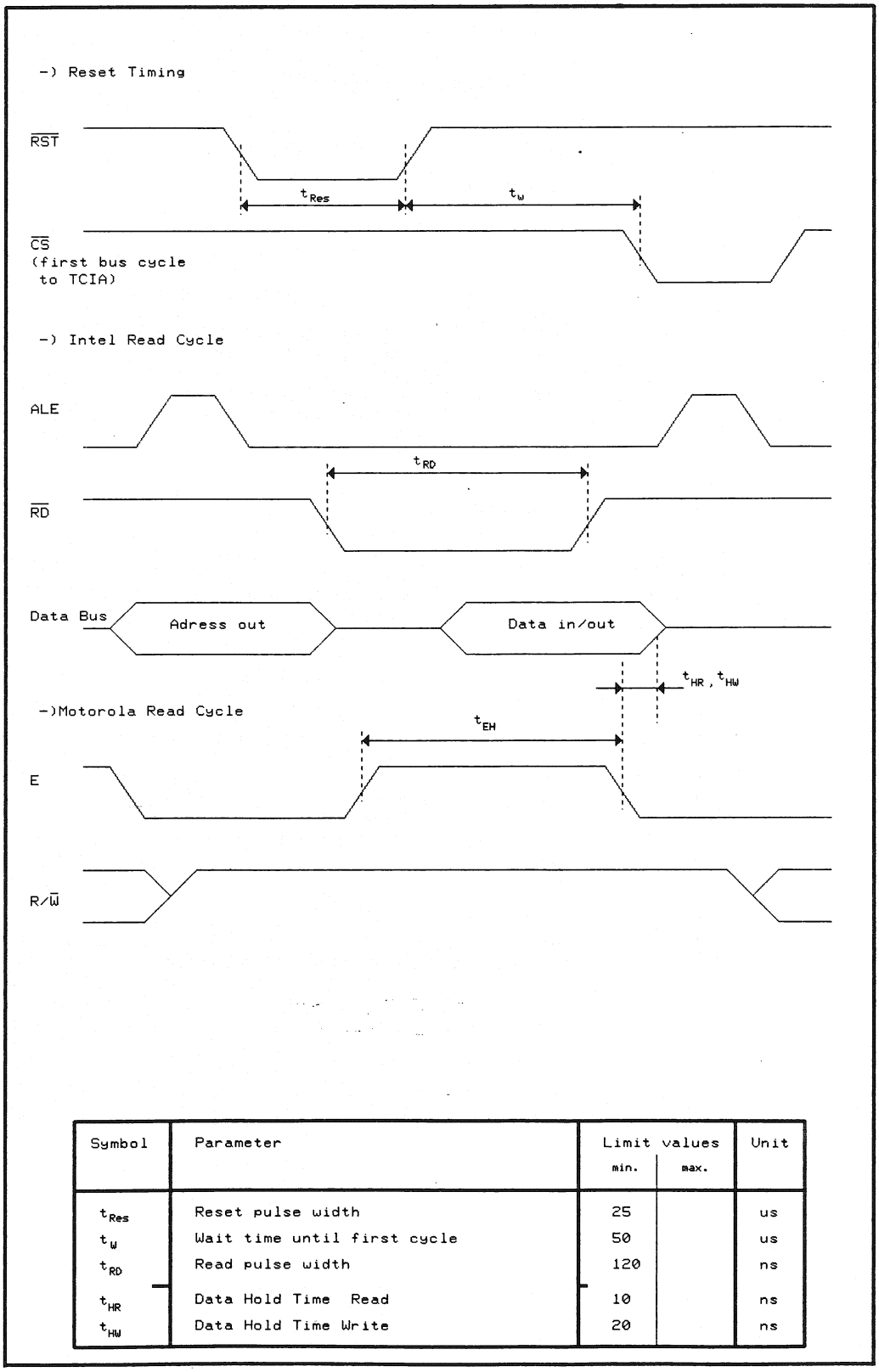
TC - SYNC is a TTL compatible active "high" output. The TC - SYNC output remains "high" during the two Time Code Clock Periods after the Sync Word has been read completely.

TC UP/DWN Time Code Direction

TC UP/DWN is a TTL compatible output used to indicate the direction of the incoming Time Code Signal. The "high" level at this output indicates the reverse direction, the "low" level the forward direction of the Time Code.

TC - VALID Time Code Valid

TC - VALID is a TTL compatible output which indicates that a valid Time Code Data is present at the TC - DATA output (active "high").



Symbol	Parameter	Limit values min.	Limit values max.	Unit
t_{Res}	Reset pulse width	25		us
t_w	Wait time until first cycle	50		us
t_{RD}	Read pulse width	120		ns
t_{HR}	Data Hold Time Read	10		ns
t_{HW}	Data Hold Time Write	20		ns

Fig. 5

5. Example for an interrupt subroutine

(all TCIA interrupt sources are enabled)

6803 assembler on HP 64000

```
IRQ     LDAA    STATUS      load TCIA status register
        TAB
        ANDA    #01100011B
        BNE     $+3         if it was a TCIA interrupt
*                           request,jump to next part;
        RTI                 else leave interrupt subroutine
*
        TBA                 load status into Akku A again
        ANDA    #00000010B
        BEQ     $+5         jump next part of interrupt
*                           routine,if it was not Receive
*                           Buffer Overrun
        LDAA    FRAME       if it was Receive Buffer
*                           Overrun,then read the Frame
*                           Buffer
        RTI                 and leave subroutine
*
        TBA                 load status again into Akku A
        ANDA    #00000001B
        BNE     $+3         if it was neither Overrun nor
*                           Underrun Interrupt Request,
*                           then jump to next part of
*                           of interrupt subroutine
*                           (a correct FRAME is received)
        RTI                 if it was Overrun or Underrun
*                           interrupt Request,then leave
*                           the subroutine now
*
        LDAA    #0FFH       set flag for main program
        STAA    FLAG        that the Time Code Data Buffers
*                           were read
        LDX     #STORE
        LDAA    HOUR        read Time Code Data Buffers
        STAA    0,X         (Frame at the end)
        LDAA    MIN         and store them
        STAA    1,X
        LDAA    SEC
        STAA    2,X
        LDAA    FRAME
        STAA    3,X
        RTI                 leave interrupt subroutine
```

6. Technical data

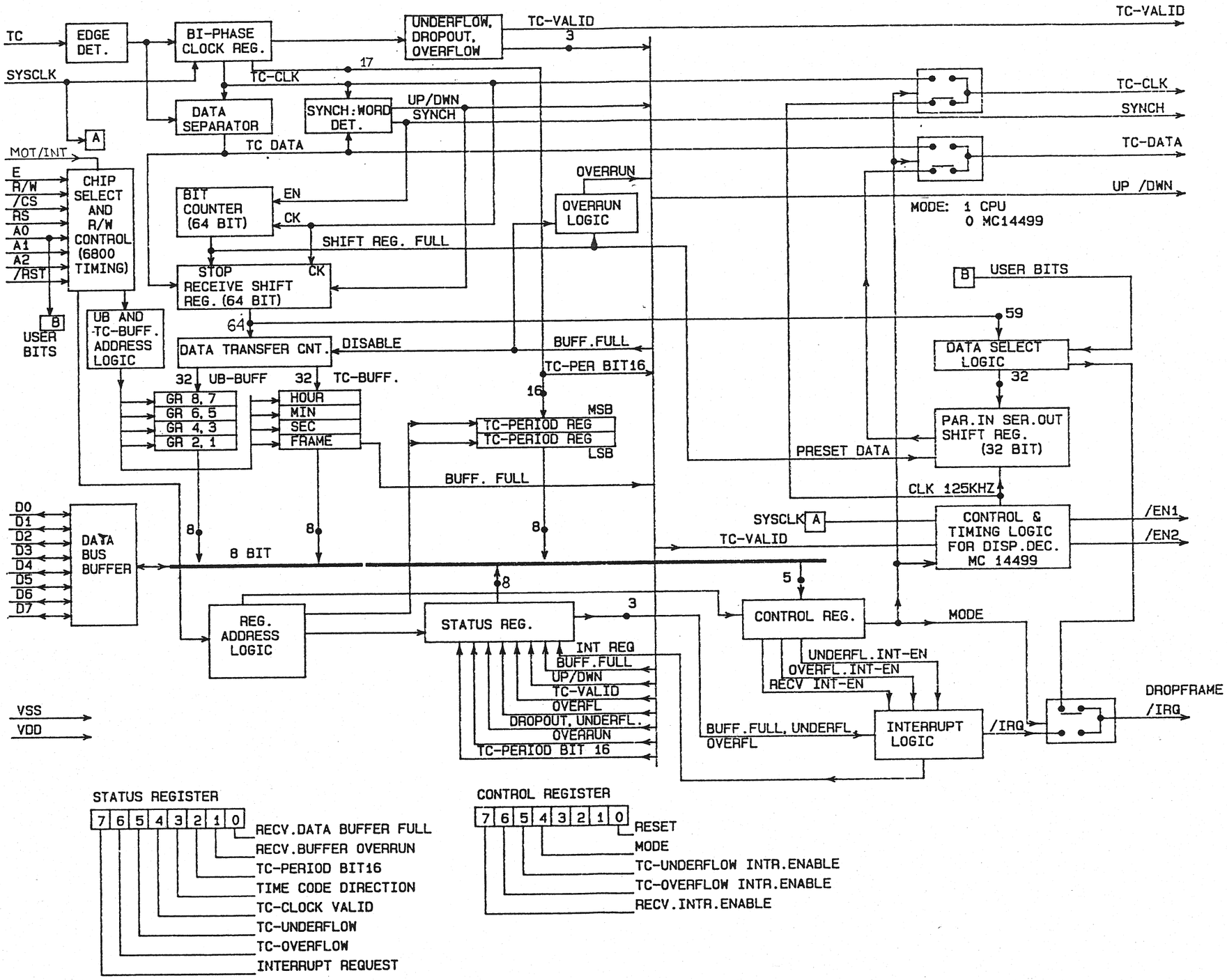
Temperature range	0 to 70 °C
Voltage on any pin with respect to ground	-0.4 to VDD +0.4V
Power supply	5V ± 10%

Symbol	Parameter		Limit values min.	typ.	max.	Unit	Test condition
VIL	Input low voltage		-0.4		0.8	V	
VIH	Input high voltage		2.0		VDD + 0.4	V	
VOL	Output low voltage				0.4	V	I_a = 4mA
VOH	Output high voltage		2.4			V	I_{OH} = 4mA
IOLH	Output current low/ high Bidir. Buffers				4	mA	
IOC	Open drain output current				12	mA	
ICC	Power supply current	operational		250		uA	VDD=5V Inputs at 0V/VDD no Output loads
		power down (no Clock)		100		uA	
ILI	Input leckage current				10	uA	
ILO	Output leckage curr.				10	uA	
C_{in}	Max input capacitance				2,5	pF	
t_R	Rise time of all outputs				5	ns	with 50pF load

- List of signals with internal pull up resistor (~50kOhm):
  E, R/$\overline{W}$, Mot/$\overline{Int}$, $\overline{CS}$, RS, A0, A1, A2, D0....D7

table 1

TCIA BLOCK DIAGRAM



STATUS REGISTER

7	6	5	4	3	2	1	0

- RECV.DATA BUFFER FULL
- RECV.BUFFER OVERRUN
- TC-PERIOD BIT16
- TIME CODE DIRECTION
- TC-CLOCK VALID
- TC-UNDERFLOW
- TC-OVERFLOW
- INTERRUPT REQUEST

CONTROL REGISTER

7	6	5	4	3	2	1	0

- RESET
- MODE
- TC-UNDERFLOW INTR.ENABLE
- TC-OVERFLOW INTR.ENABLE
- RECV.INTR.ENABLE

EDITION: 6. November 1989